

Compal Confidential

PEW52 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

2010-08-06

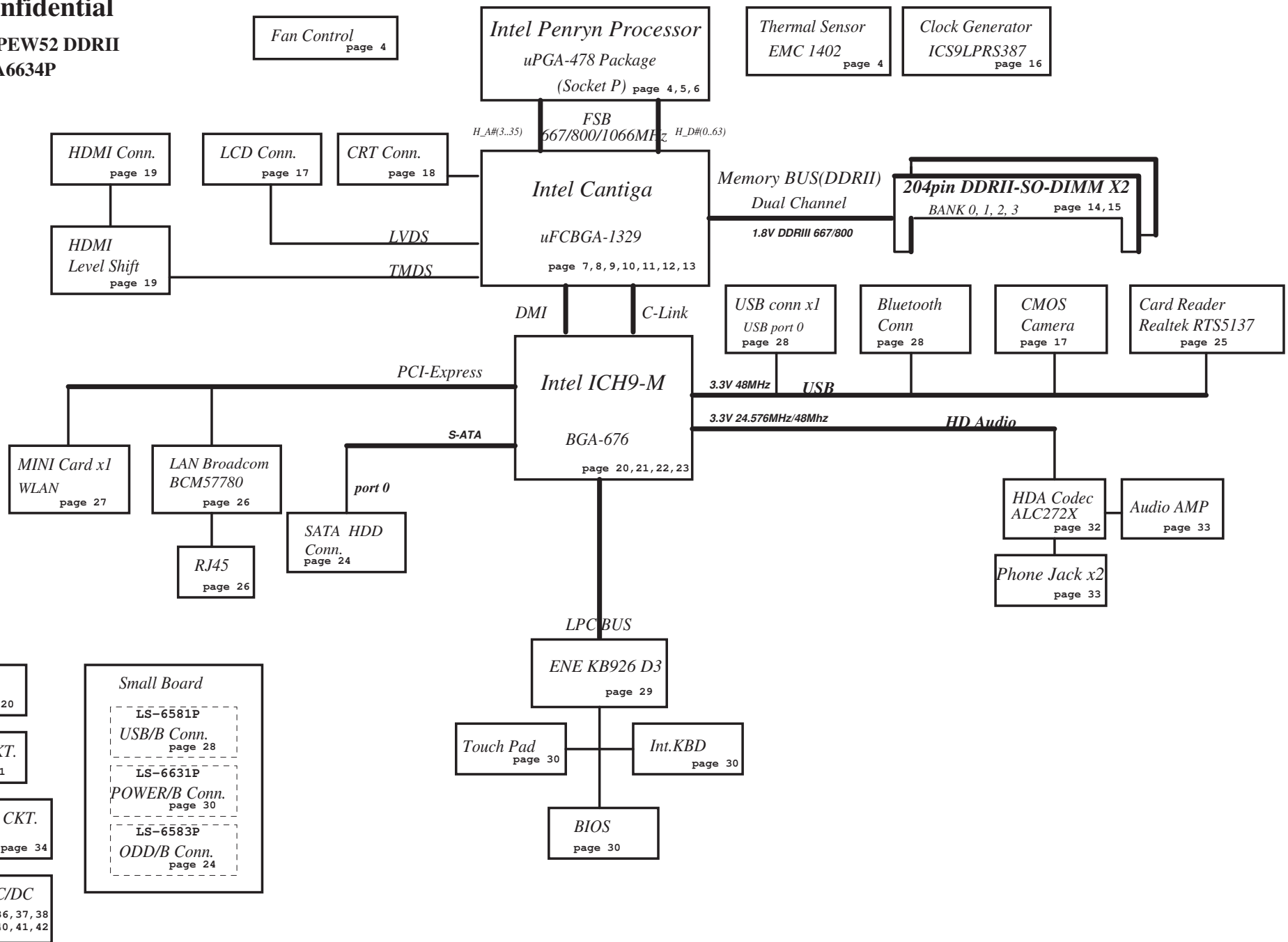
REV : 0 . 1

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Model Name : PEW52 DDRII

File Name : LA6634P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for LVDS	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	SMSC EMC1402	100 1100 b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LVRS367, RTM890N)	1101 001Xb
DDR DIMM1	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
GM45 B3	GM@
GM40 A1	GLA1@
Bluetooth	BT@

PCIe table

PCIe port1	
PCIe port2	Wireless Card
PCIe port3	PCIe LAN
PCIe port4	
PCIe port5	
PCIe port6	

SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

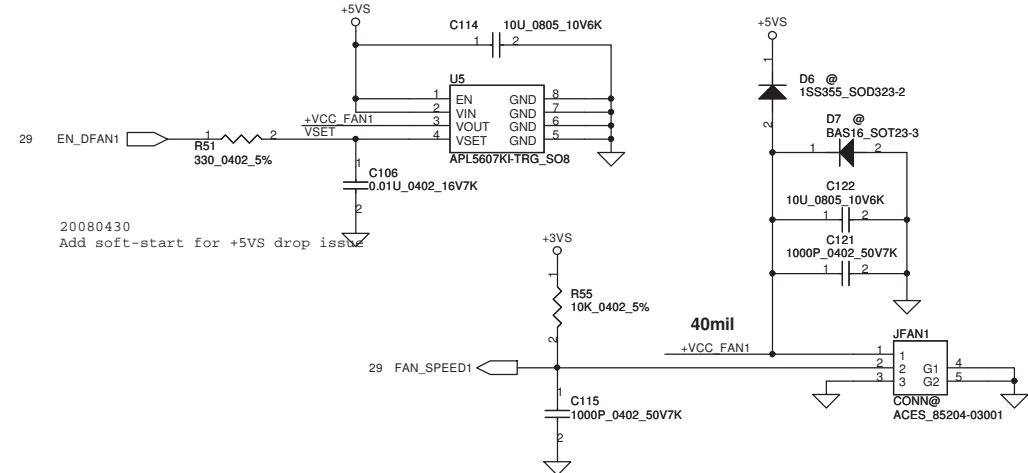
USB table

EHCI1	UHCI1	Port0	MB USB Conn.
		Port1	USB/B Conn.
	UHCI2	Port2	
		Port3	CMOS Camera
	UHCI3	Port4	Card Reader
Port5			
EHCI2	UHCI4	Port6	USB/B Conn.
		Port7	
	UHCI5	Port8	Blue Tooth
		Port9	
	UHCI6	Port10	Wireless Card
Port11			

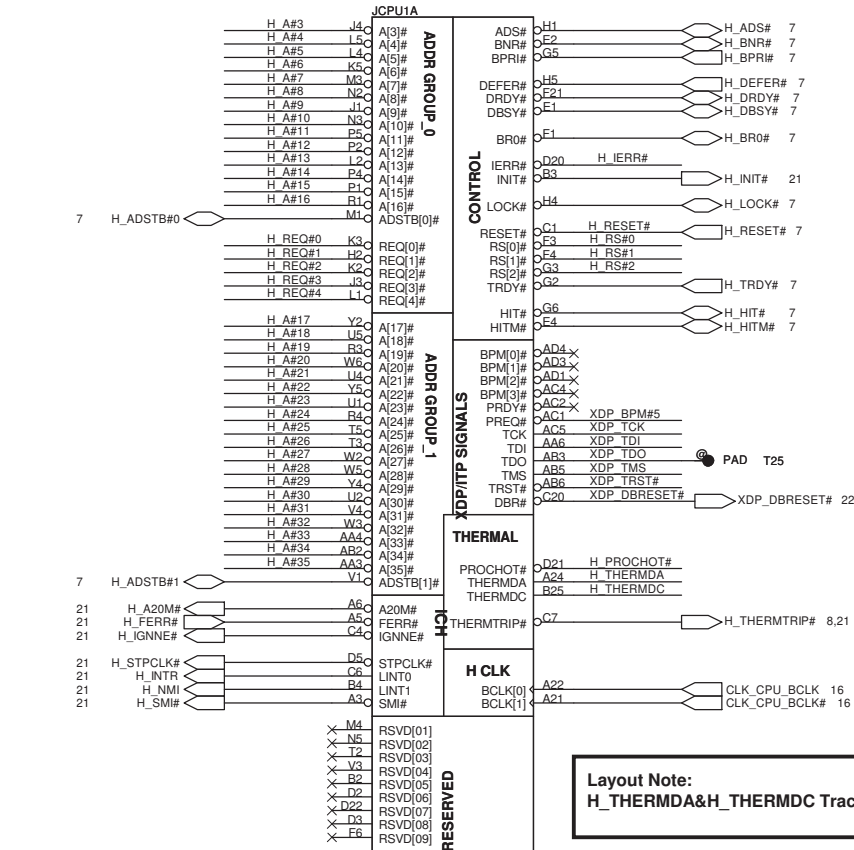
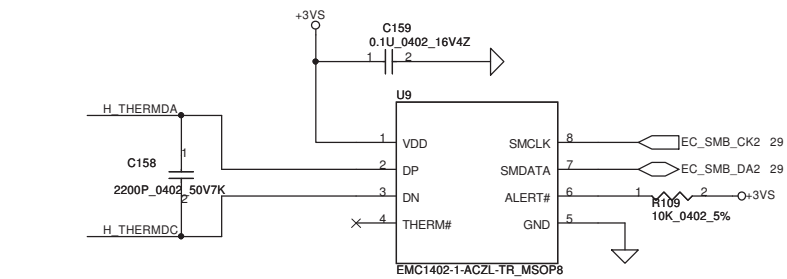
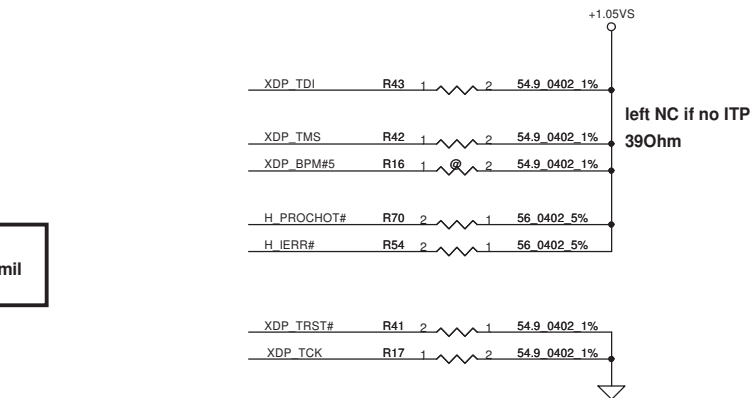
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7 H_A#[3..35] H_A#[3..35]
 7 H_REQ#[0..4] H_REQ#[0..4]
 7 H_RS#[0..2] H_RS#[0..2]

FAN1 Conn



20080430
 Add soft-start for +5VS drop issue



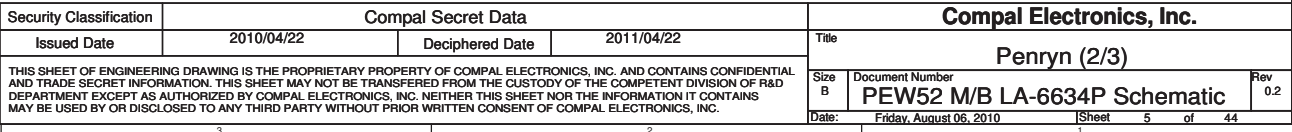
Layout Note:
 H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

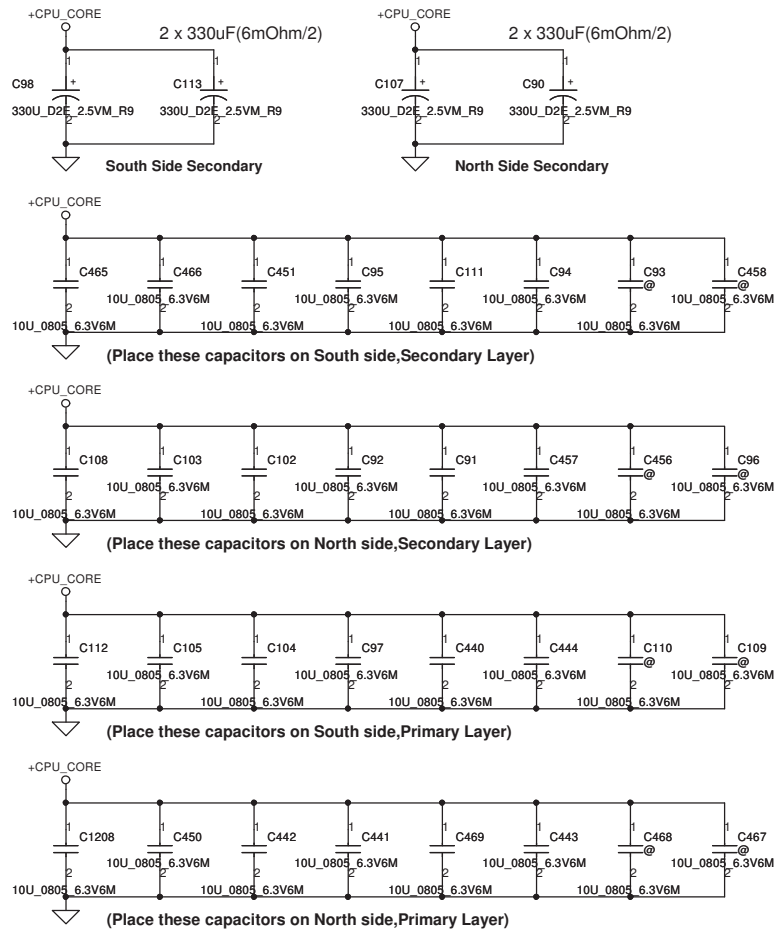
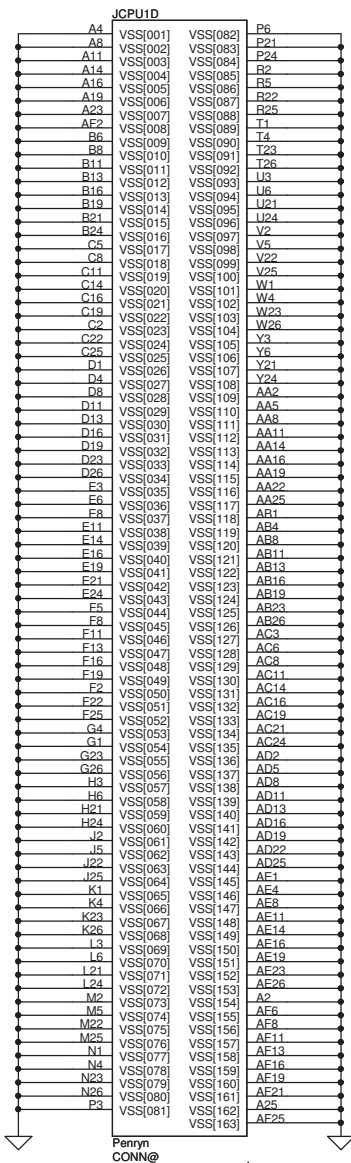
BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

PCB
 777
 LA-6634P MB Rev0: DA60000JS00
 LA-6634P MB Rev1: DA60000JS10
 LA-6634P MB with Small Board Rev1:
 PCB PEW72 LA-6631P LS-6631P/6581P/6583P

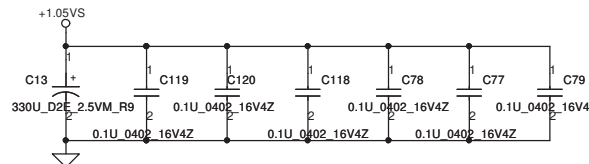
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3				2							

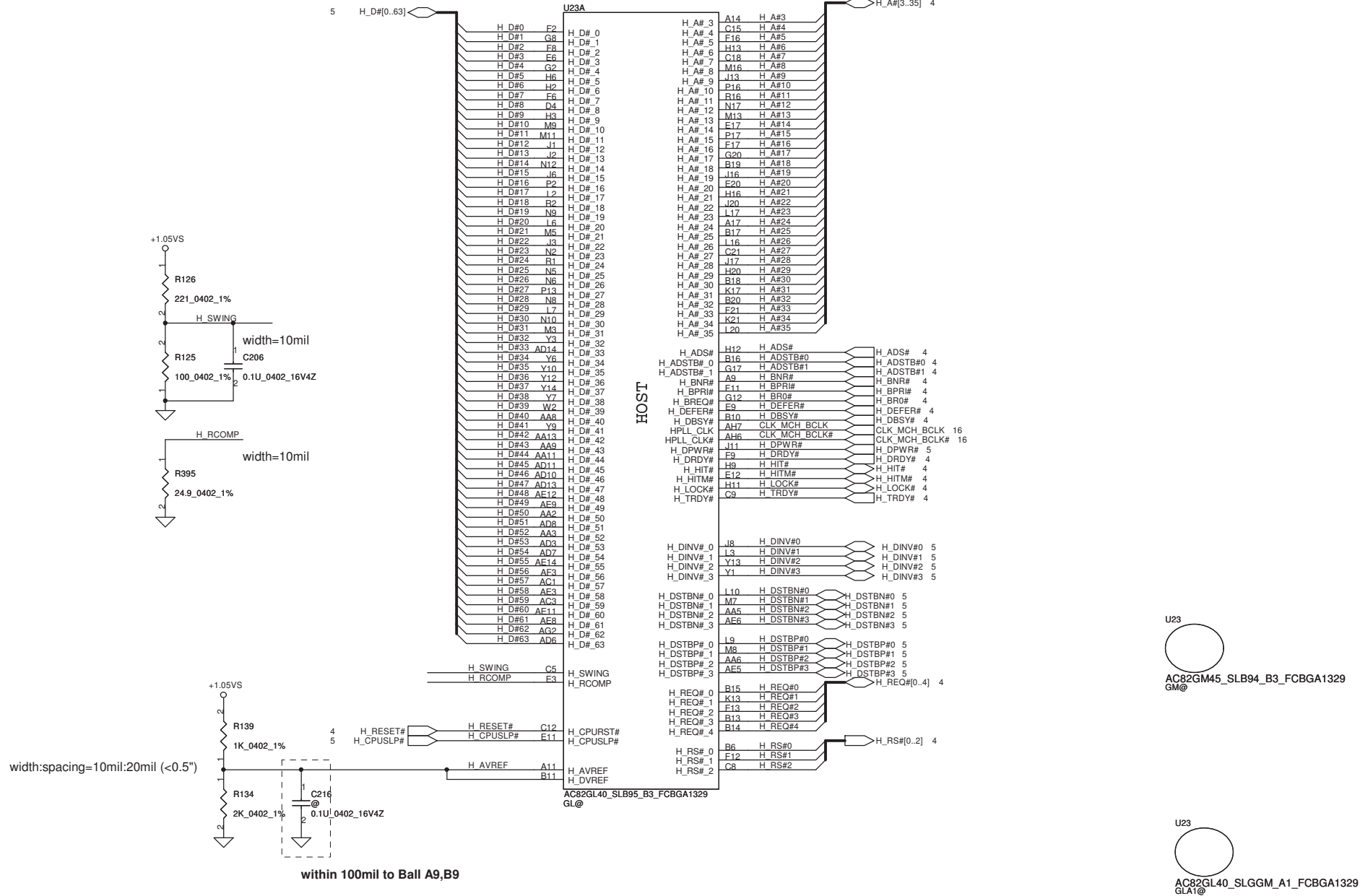




+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32

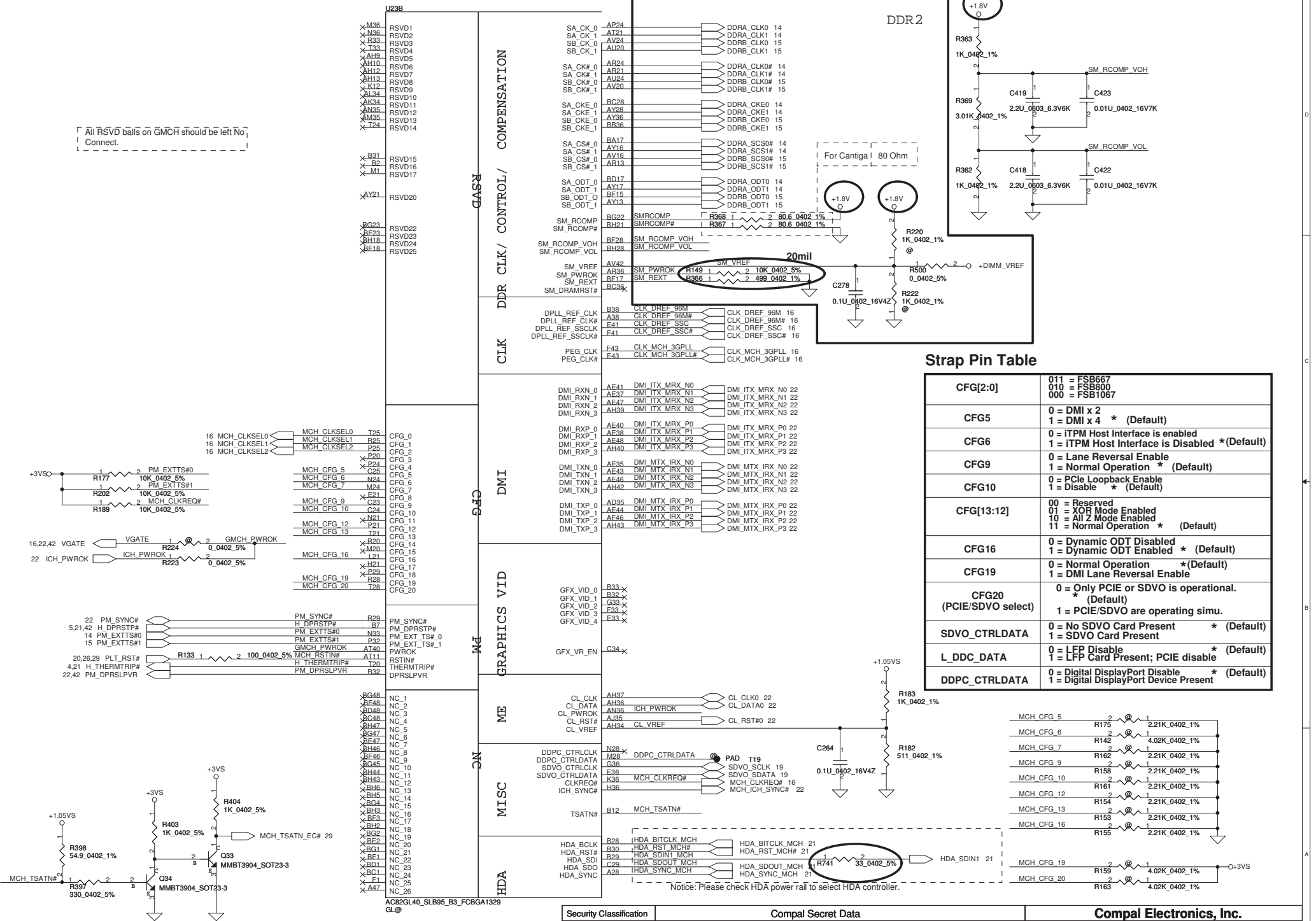


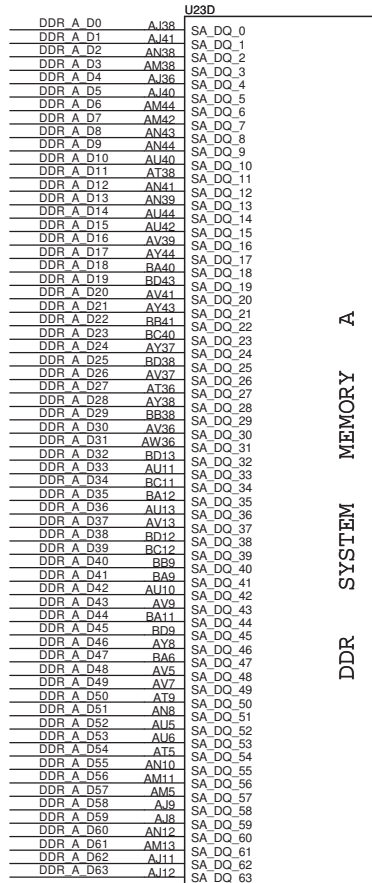
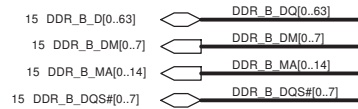
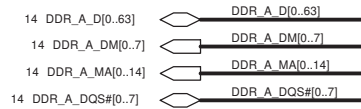
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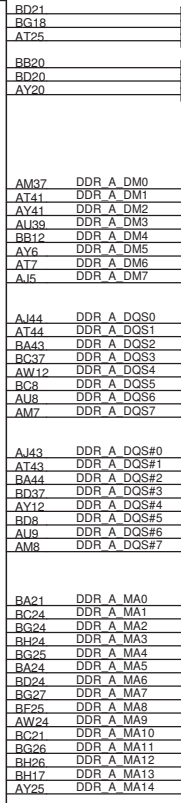
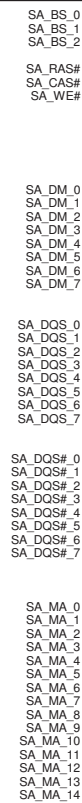
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All RSVD balls on GMCH should be left No Connect.

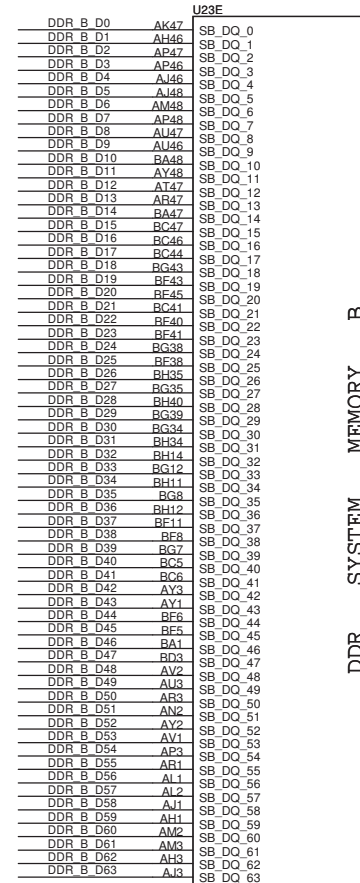




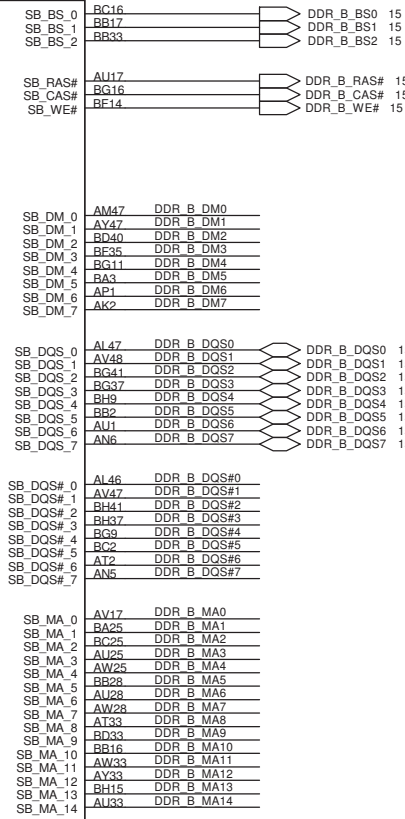
DDR SYSTEM MEMORY A



AC82GL40_SLB95_B3_FCBGA1329
GL@

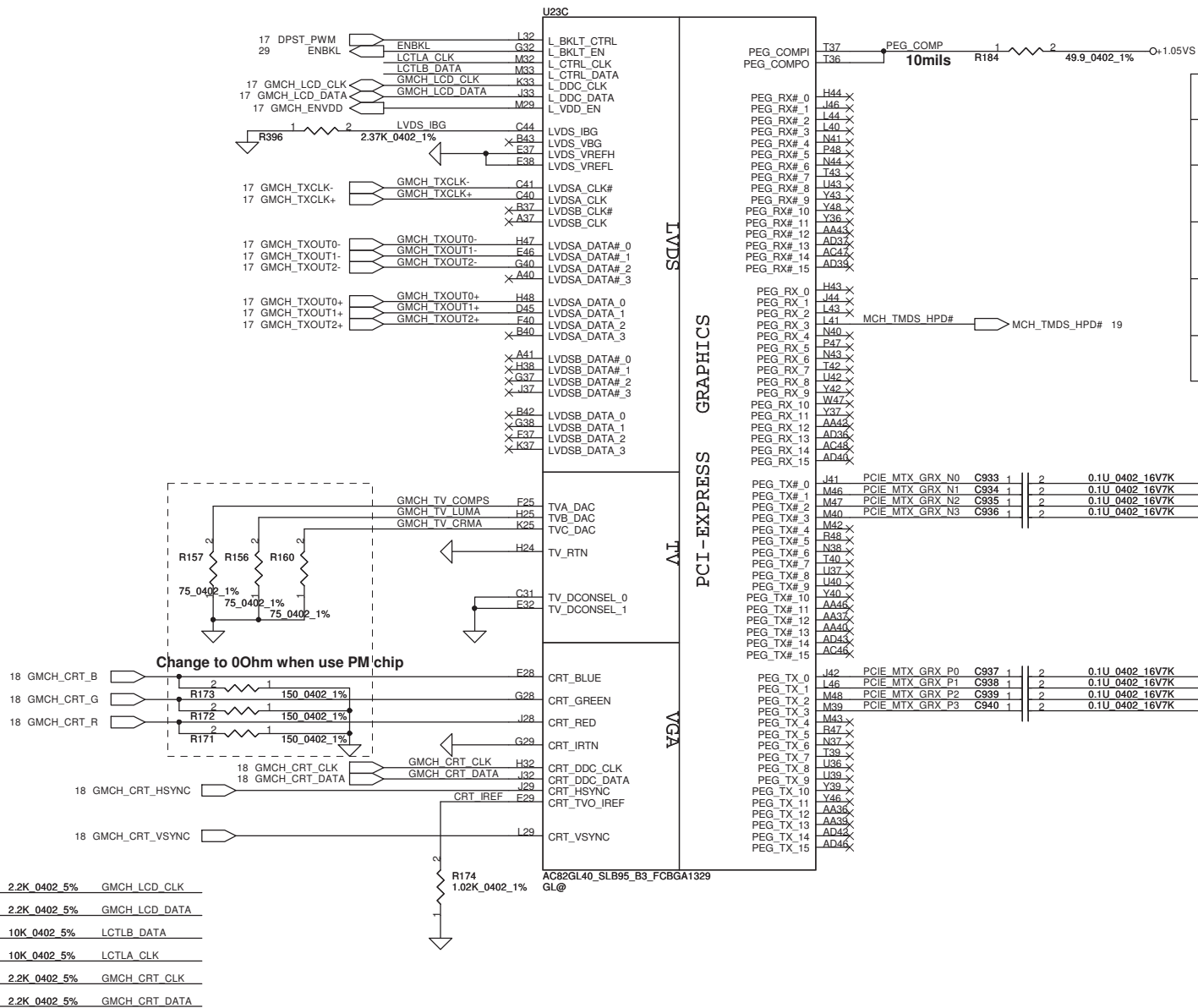


DDR SYSTEM MEMORY B



AC82GL40_SLB95_B3_FCBGA1329
GL@

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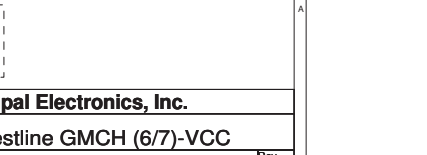
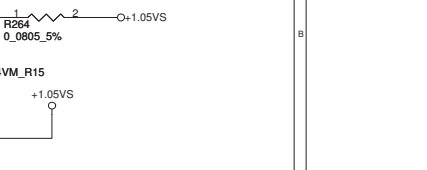
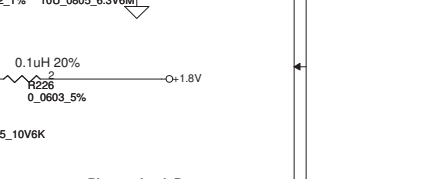
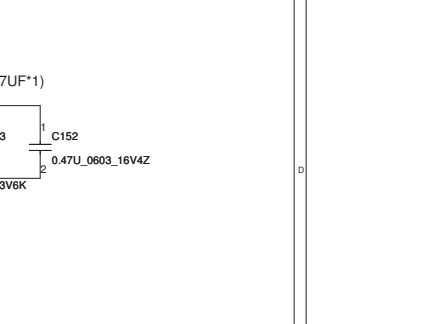
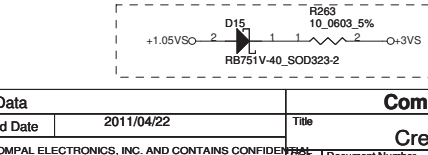
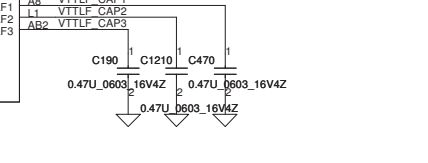
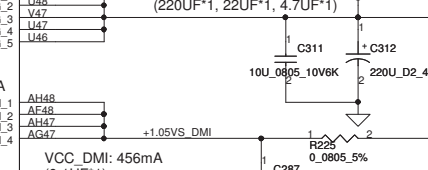
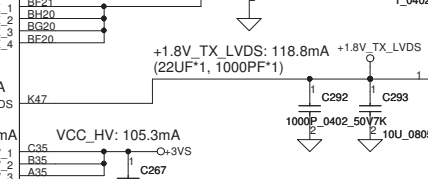
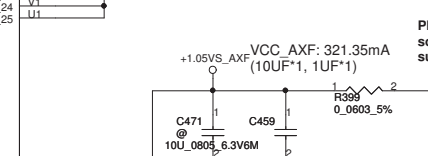
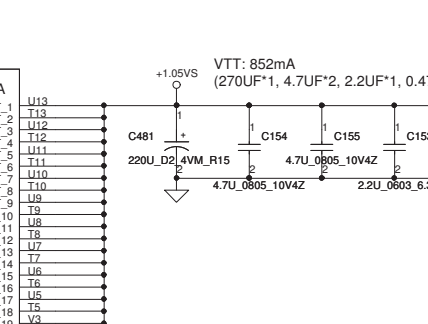
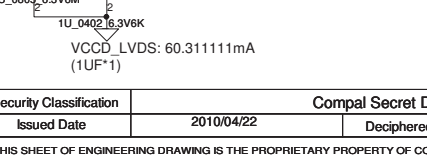
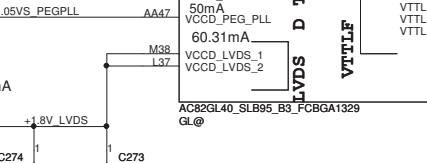
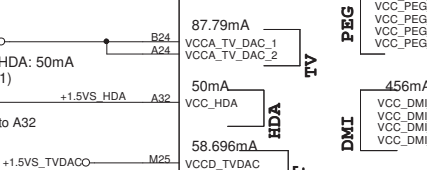
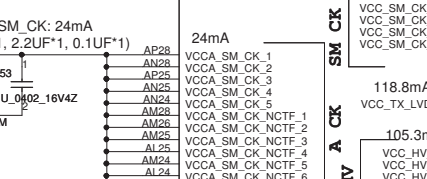
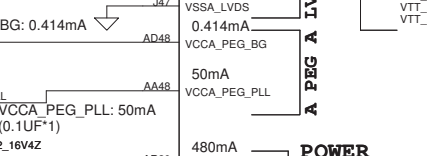
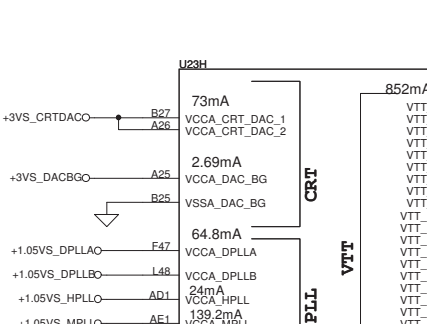
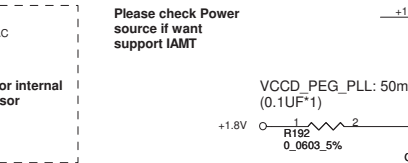
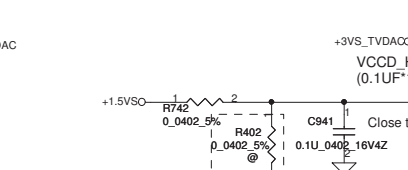
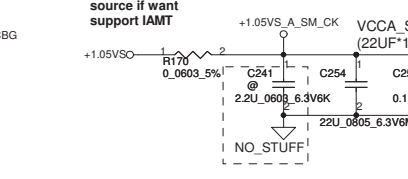
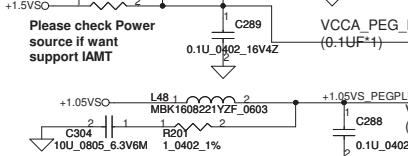
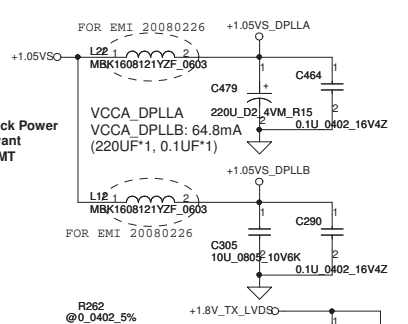
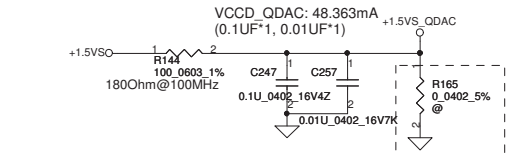
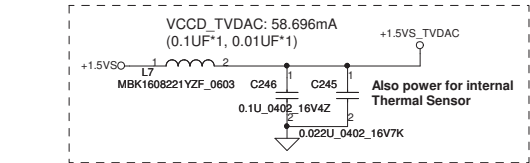
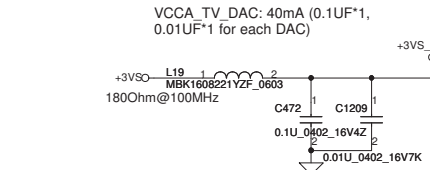
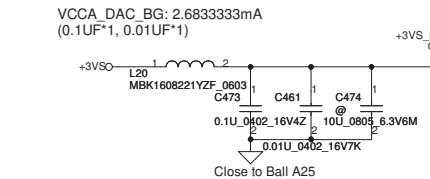
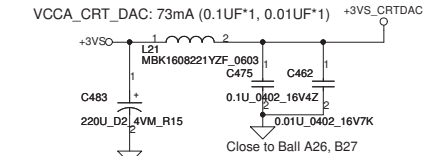
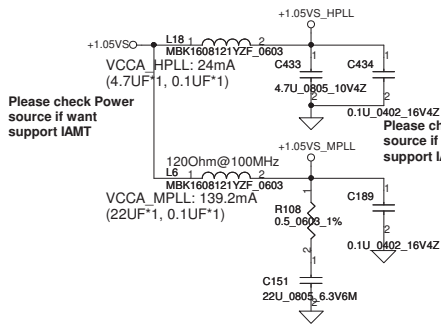


Intel Cantiga TMD5 Pin Definition

TMD5_B_CLK	PEG_TXP_3
TMD5_B_CLK#	PEG_TXN_3
TMD5_B_DATA0	PEG_TXP_2
TMD5_B_DATA0#	PEG_TXN_2
TMD5_B_DATA1	PEG_TXP_1
TMD5_B_DATA1#	PEG_TXN_1
TMD5_B_DATA2	PEG_TXP_0
TMD5_B_DATA2#	PEG_TXN_0
TMD5_B_HPDI#	PEG_RXP_3

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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

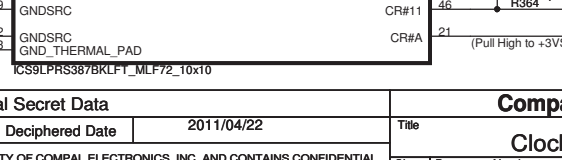
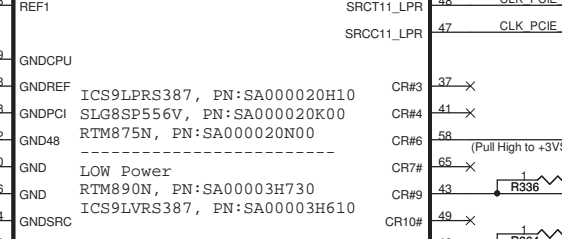
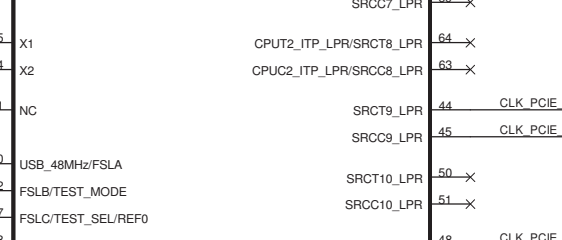
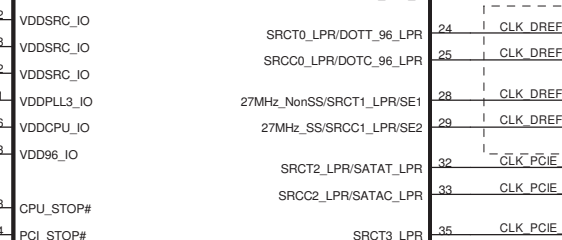
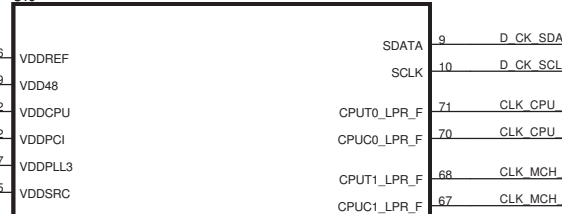
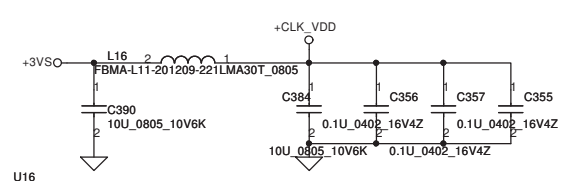
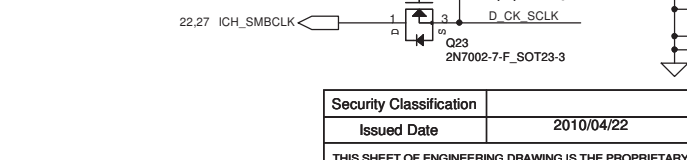
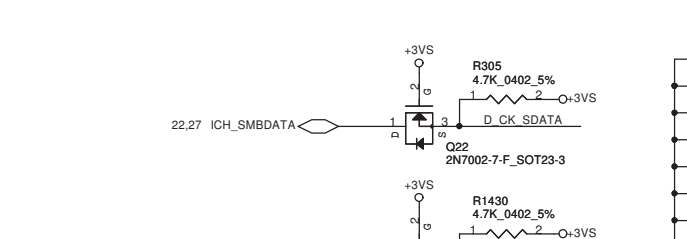
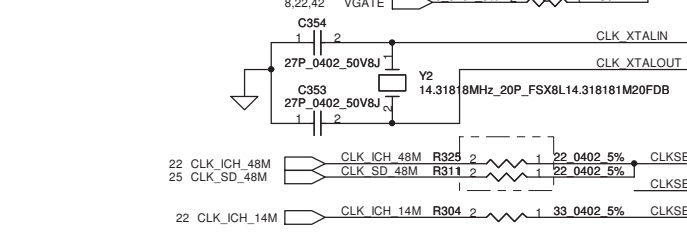
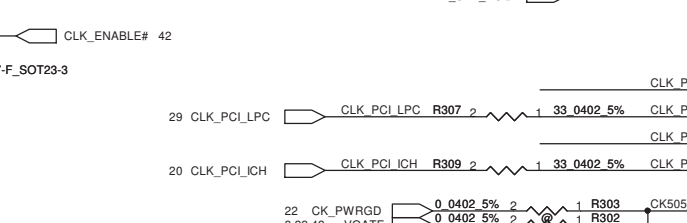
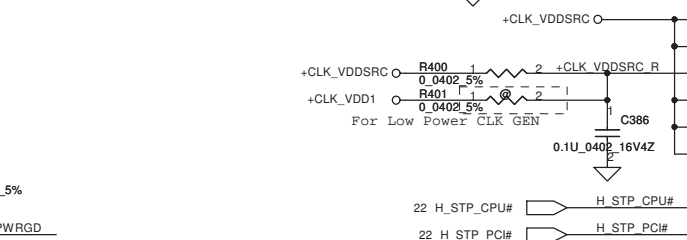
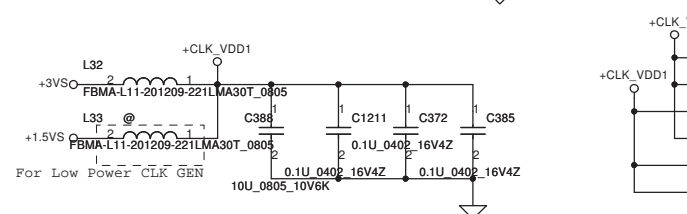
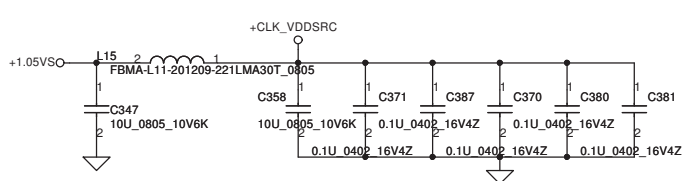
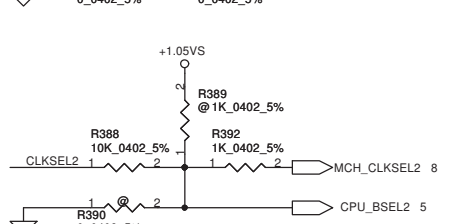
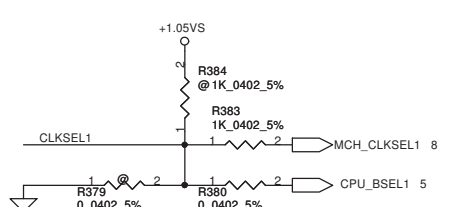
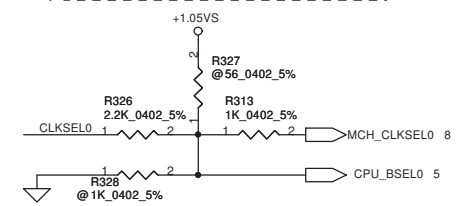
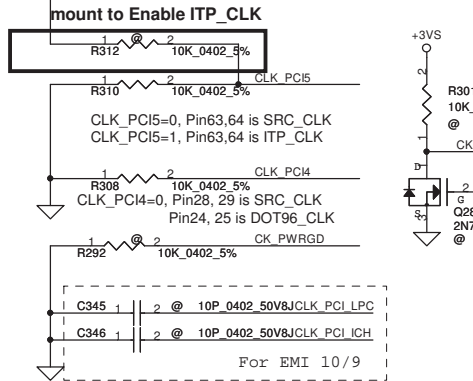
Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

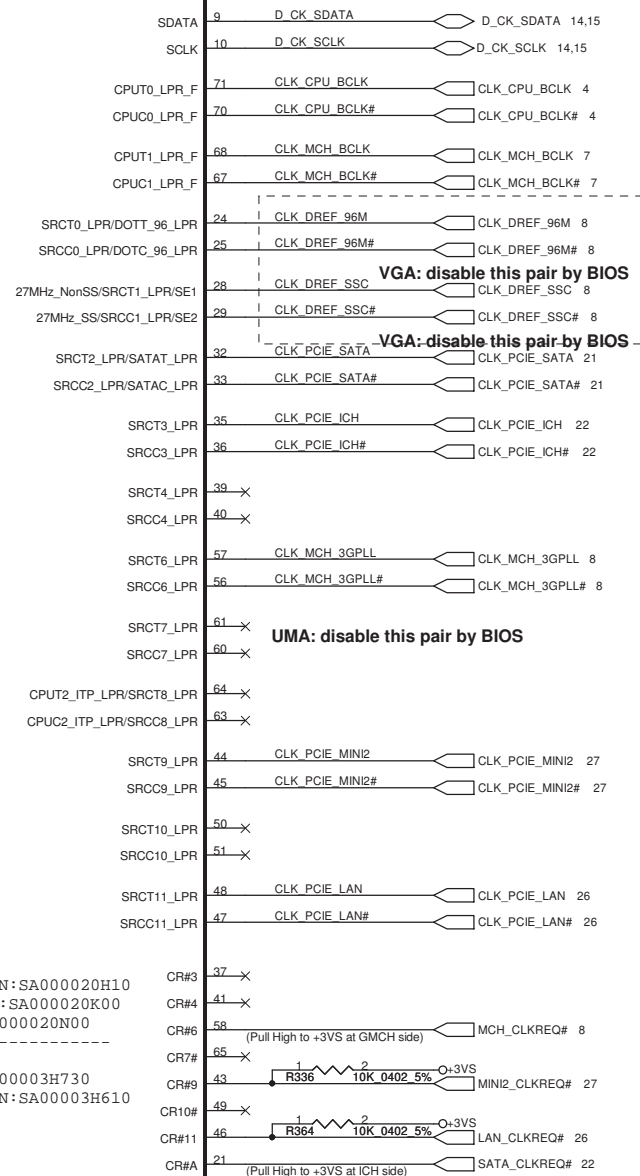
SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

+3VS CLK_PCI2=1, Trusted Mode Enable(No overlocking allowed)

mount to Enable ITP_CLK

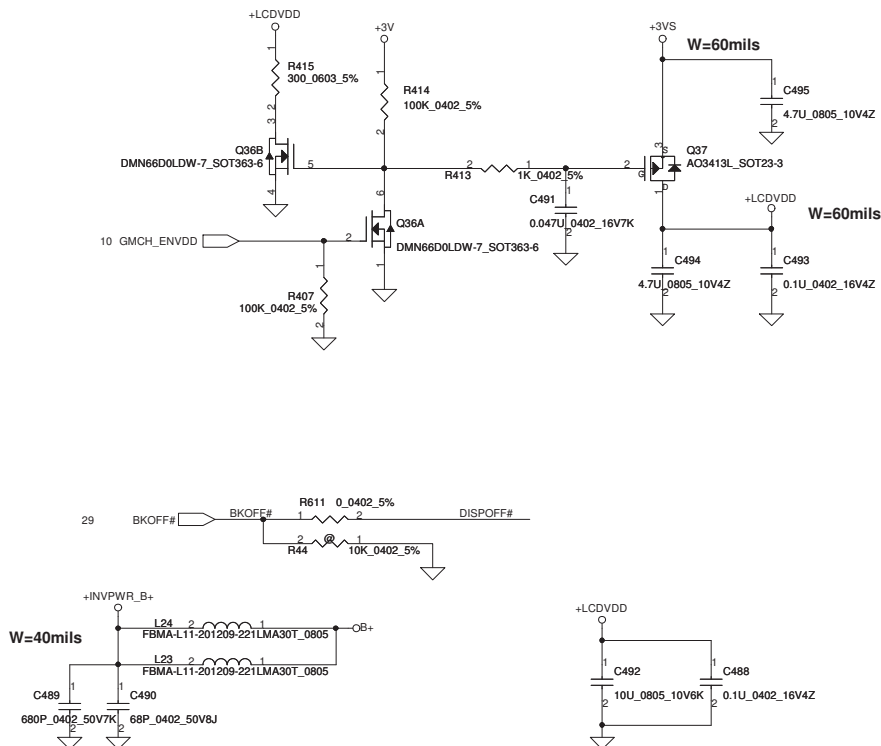


Clock Generator

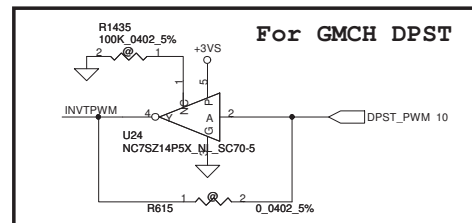
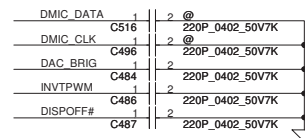
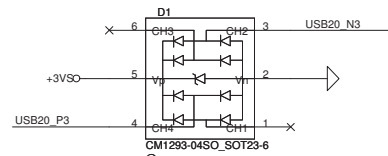
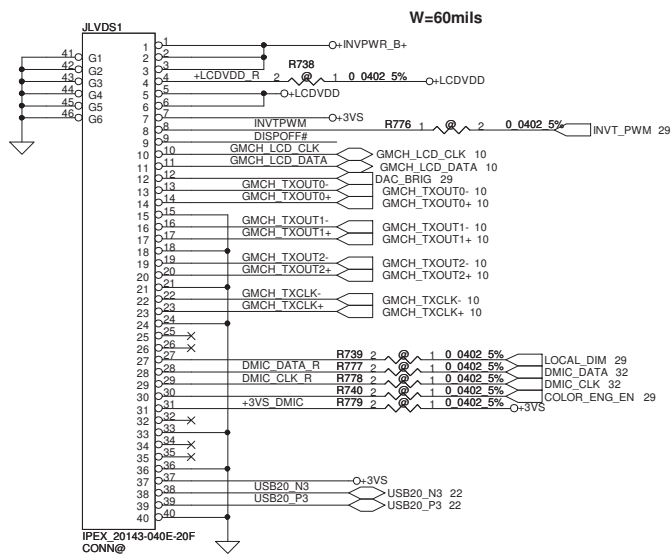


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Size	Document Number	Customer	PEW52 M/B LA-6634P Schematic	Rev	0.2
Date:	Friday, August 06, 2010	Sheet	16	of	44

LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



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				Deciphered Date				2011/04/22			
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Date				Friday, August 06, 2010				Sheet			
				17				of			
				44							

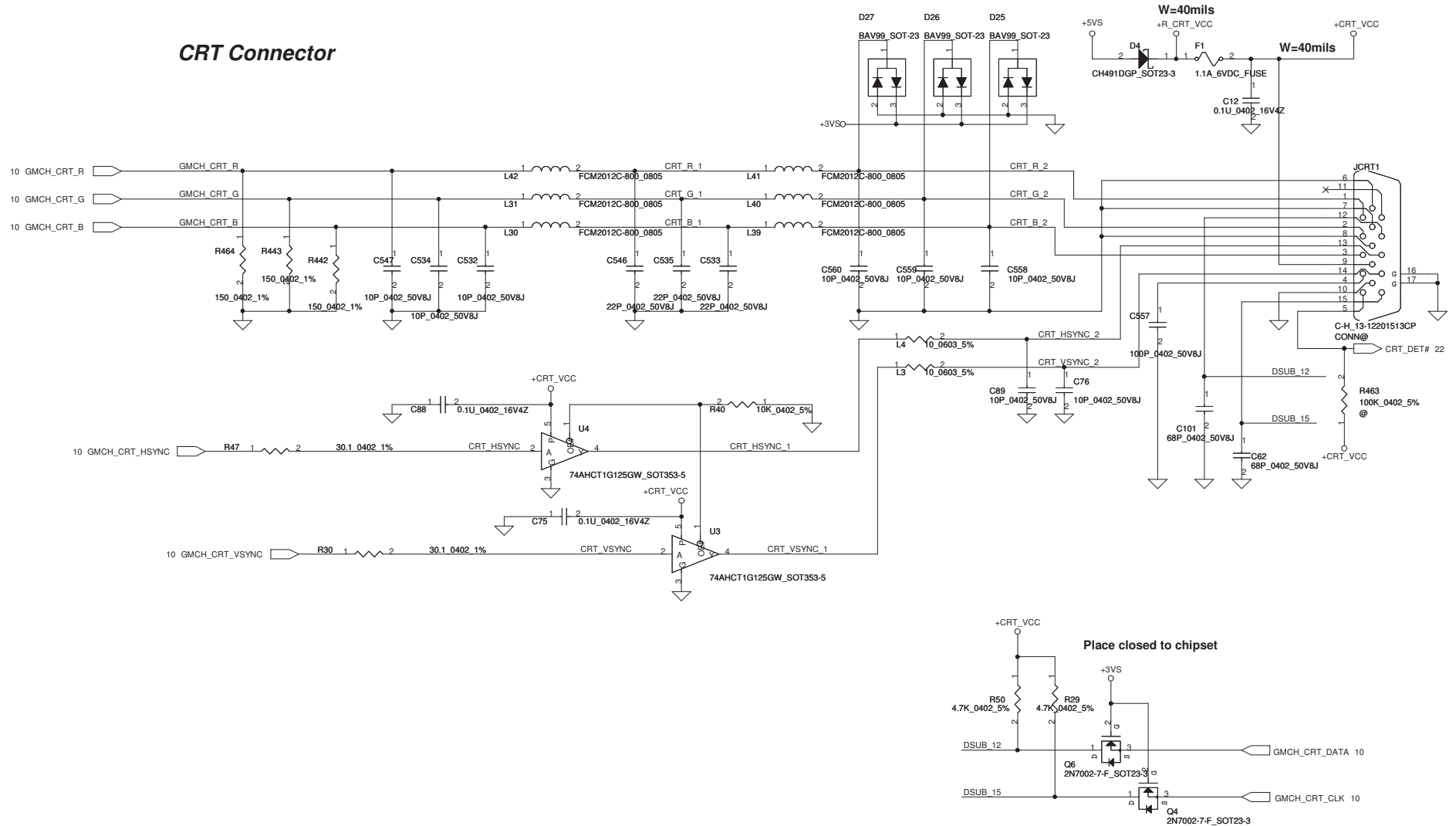
Compal Electronics, Inc.

LVDS Connector

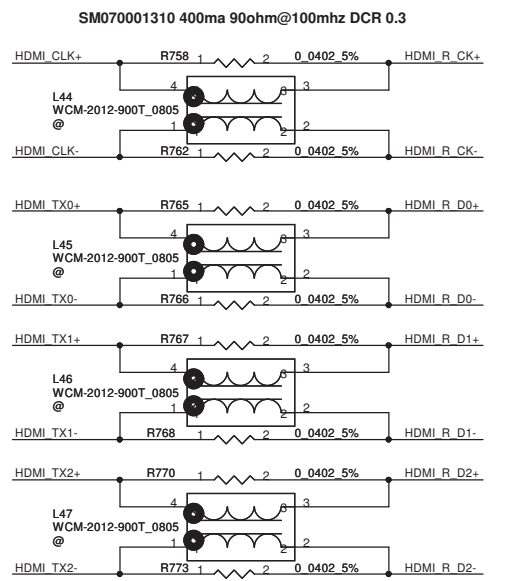
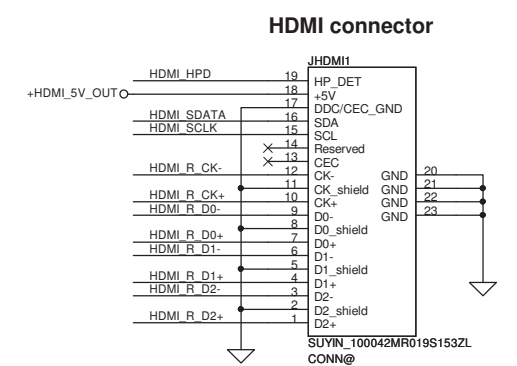
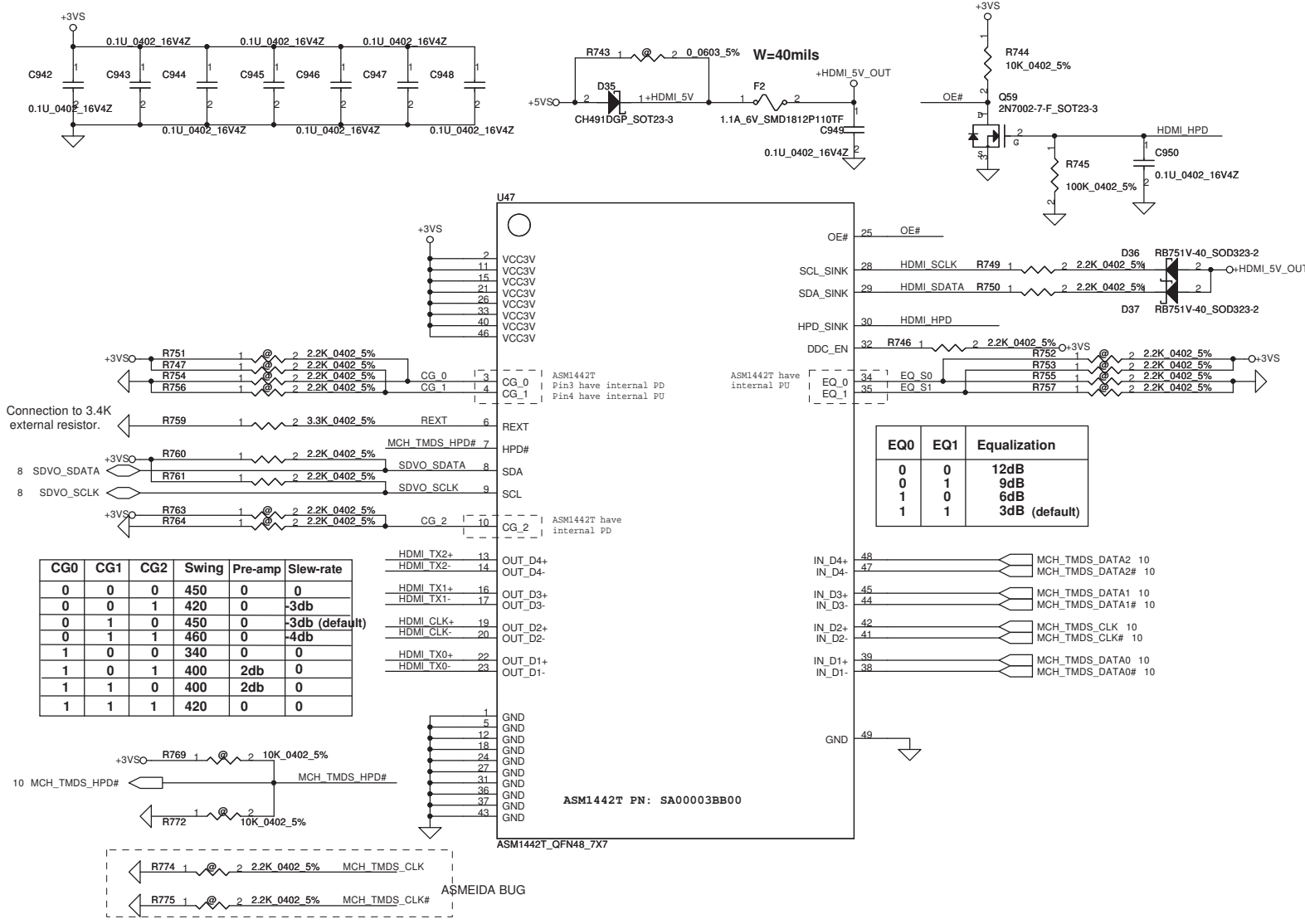
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PEW52 M/B LA-6634P Schematic

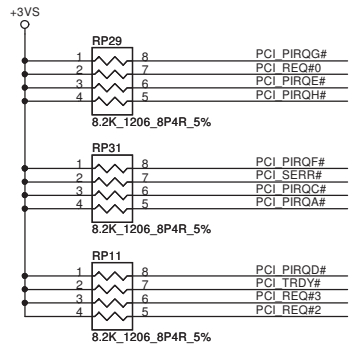
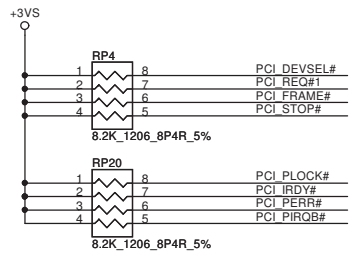
Date: Friday, August 06, 2010 Sheet 17 of 44

CRT Connector

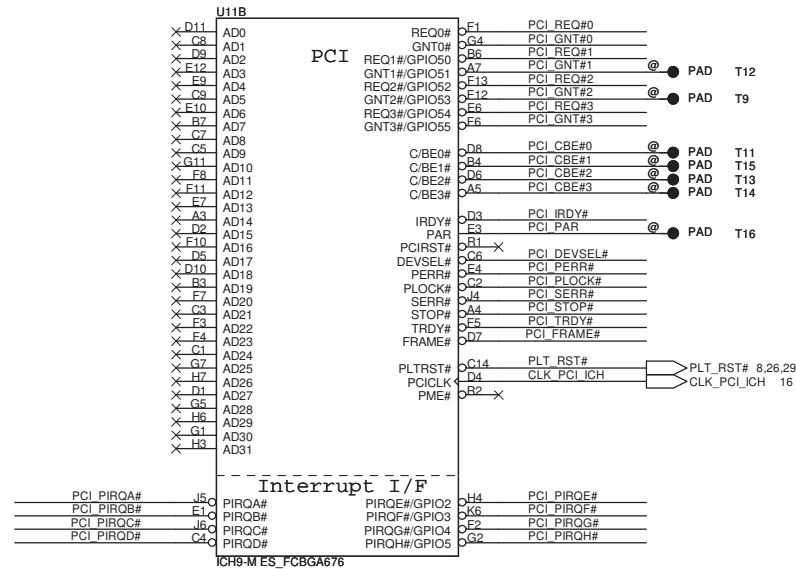


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Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title	CRT Connector
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				PEW52 M/B LA-6634P Schematic	
				Date	Friday, August 06, 2010

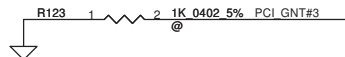




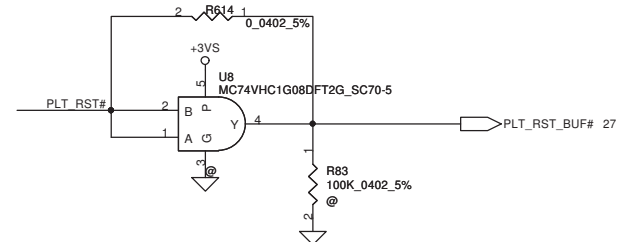
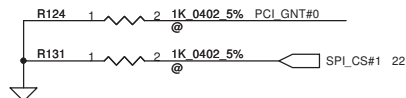
DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)



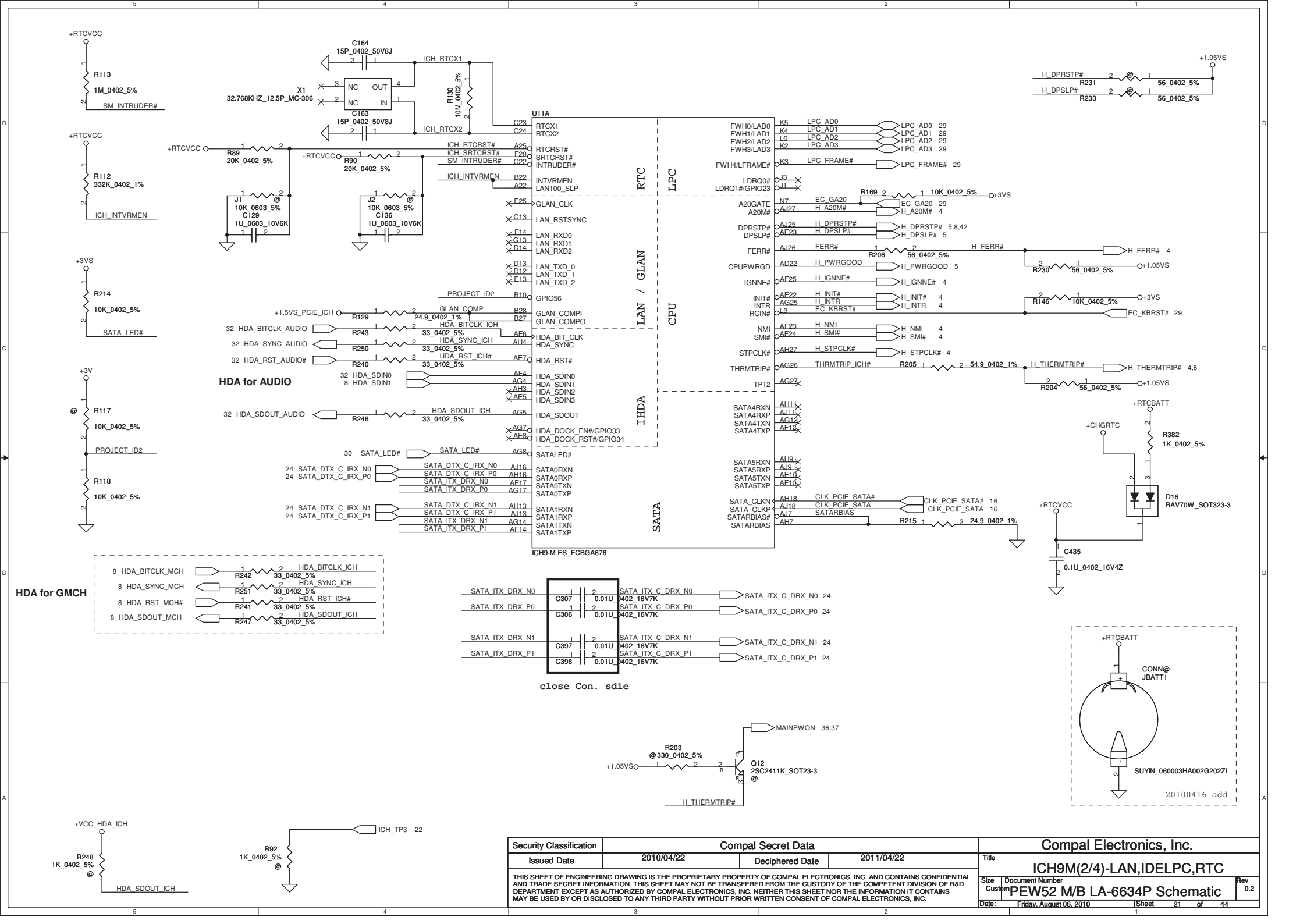
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

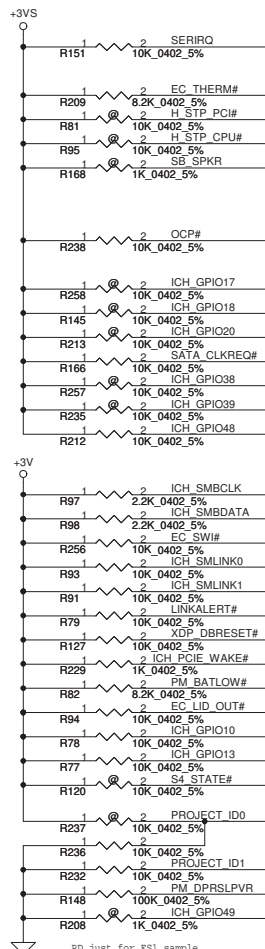


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



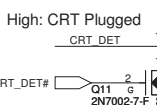
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Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title	ICH9M(1/4)-PCI
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				Date	Friday, August 06, 2010
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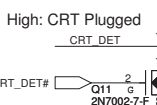


For MINI_CARD1
For PCIE LAN

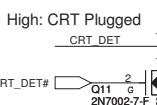
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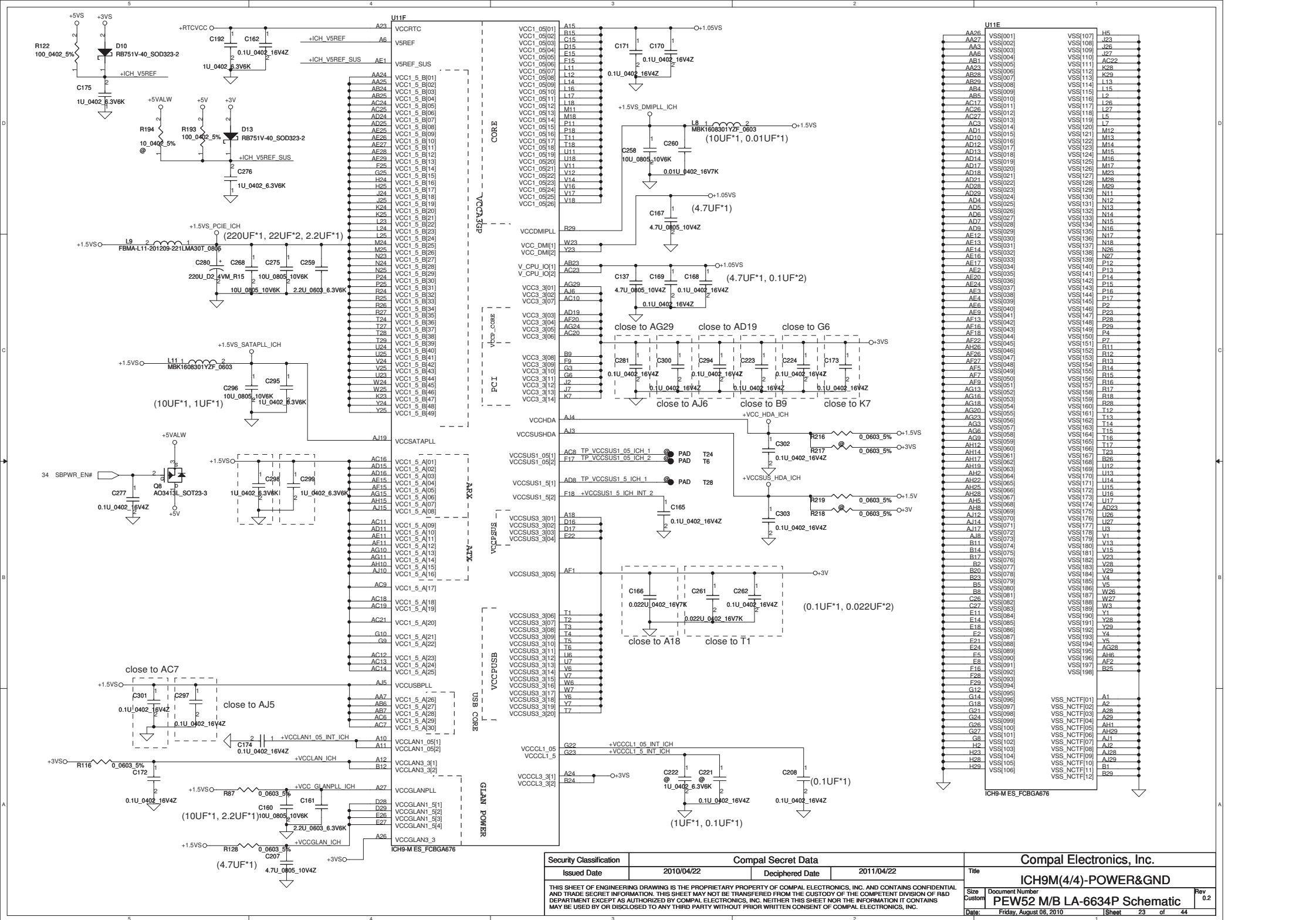


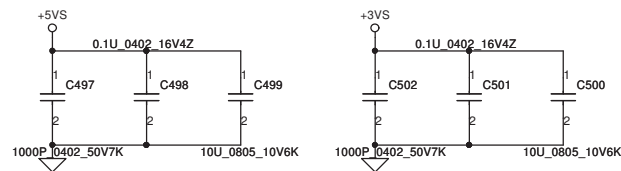
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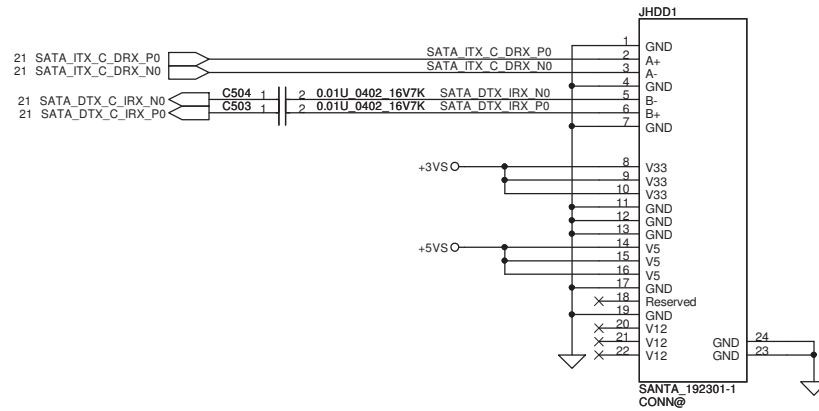
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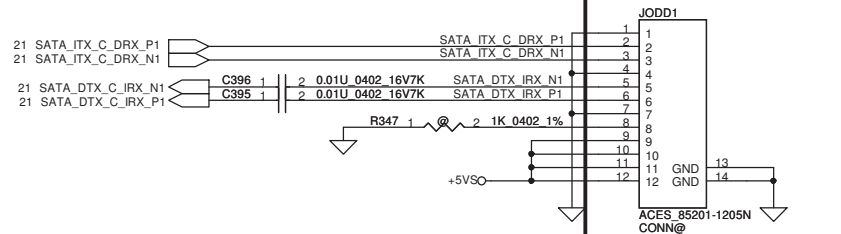




SATA HDD Conn.

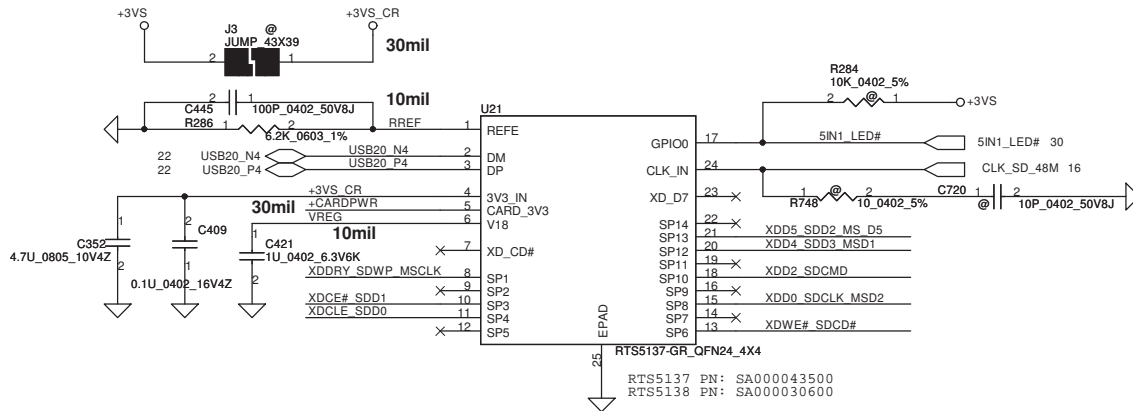


SATA ODD Conn. LS-6583

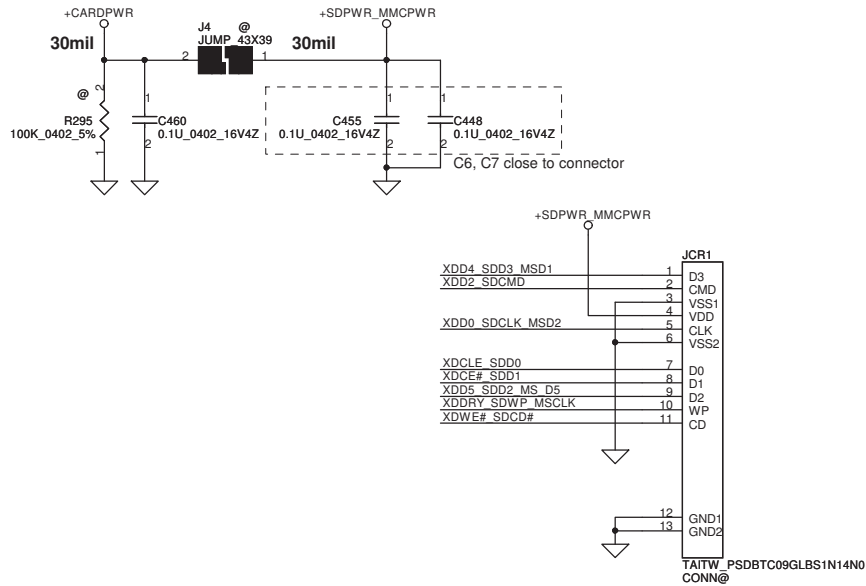


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Size	Document Number	Rev			0.2
Customer	PEW52 M/B LA-6634P Schematic				
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Card Reader RTS5138 / RTS5137
(only SD+MMC function)

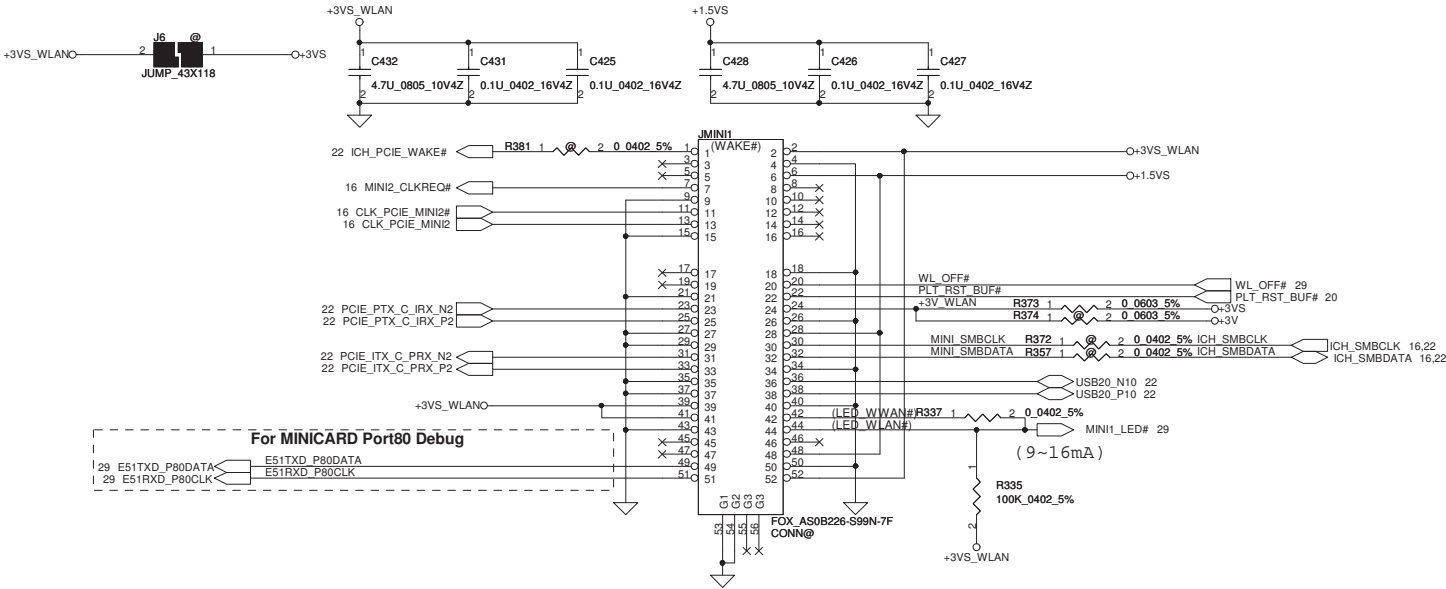


Card Reader Connector

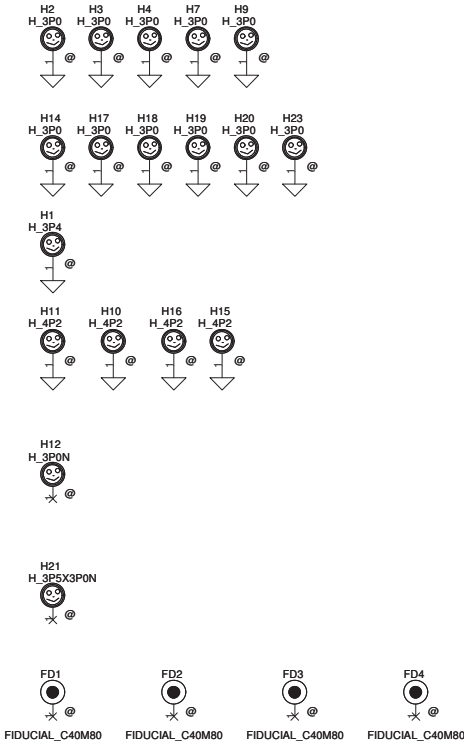


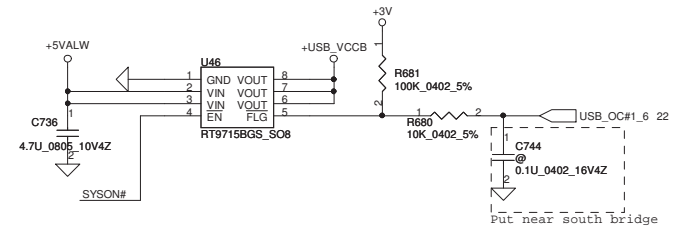
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				Customer	PEW52 M/B LA-6634P Schematic	0.2
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For Wireless LAN

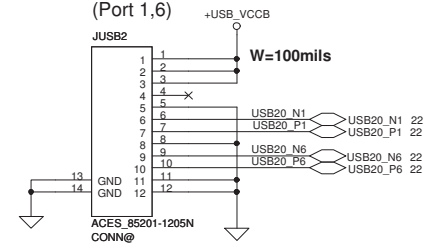


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

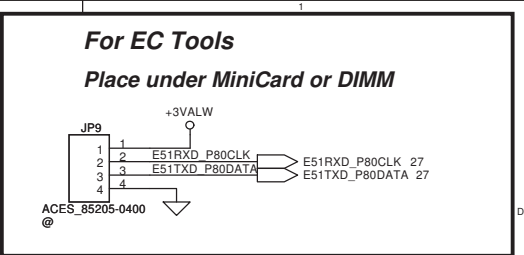


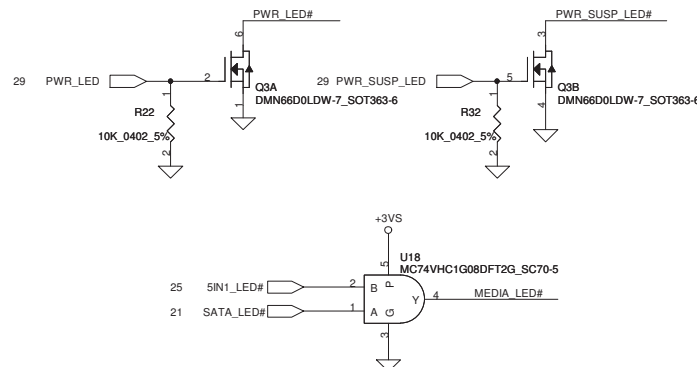
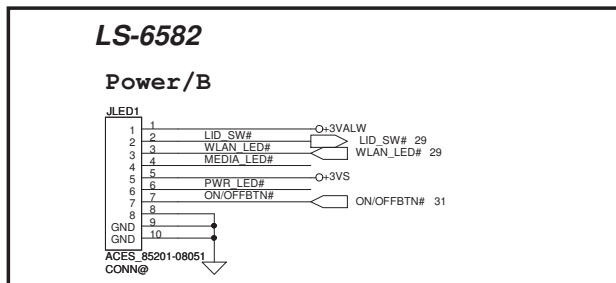
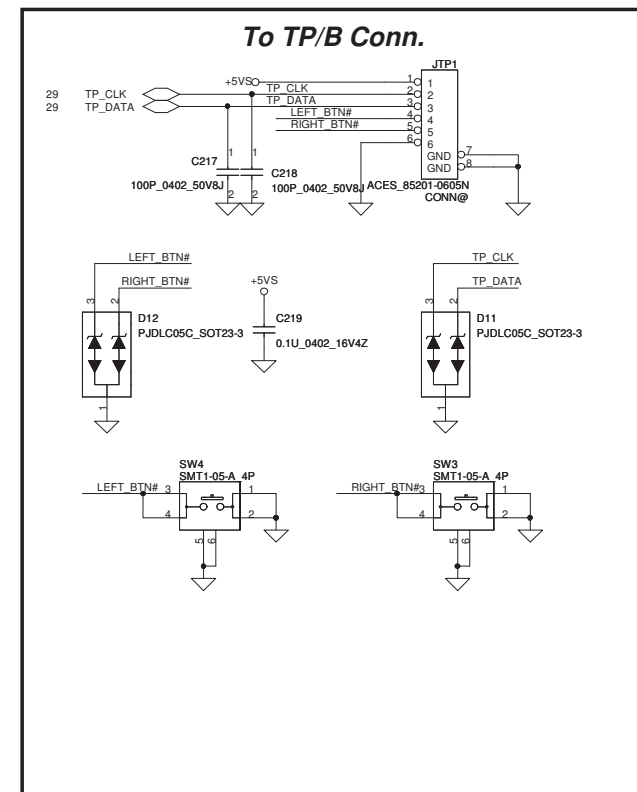


USB/B Conn. LS-6581
(Port 1,6) +USB_VCCB



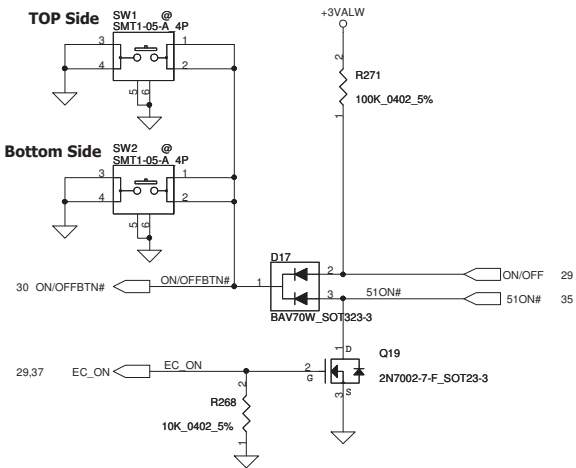
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Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title	BT & USB Connector
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				PEW52 M/B LA-6634P Schematic	
				Date	Friday, August 06, 2010



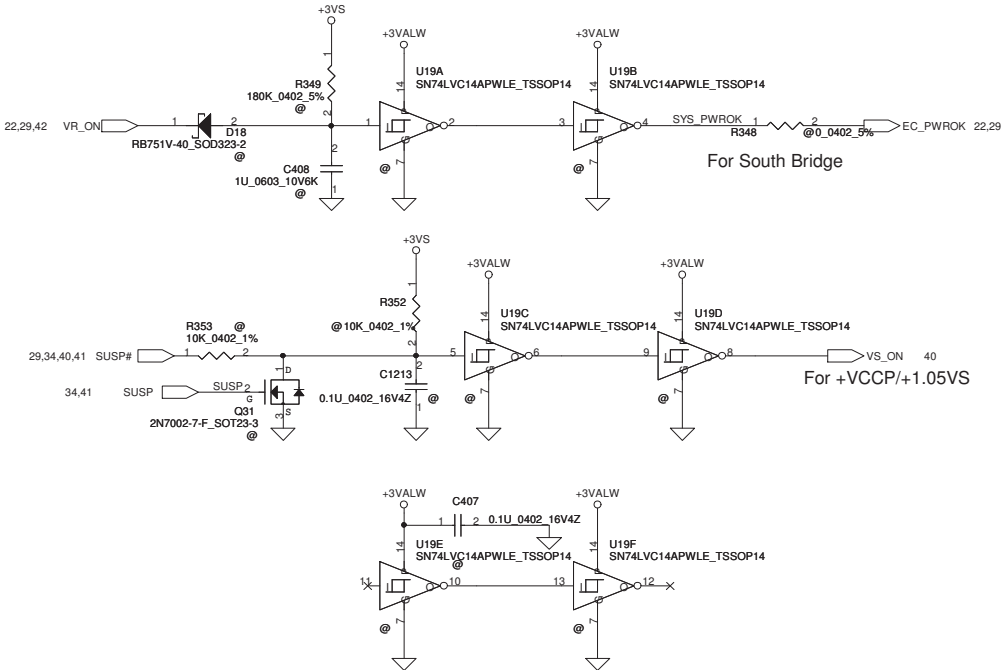


Power Button

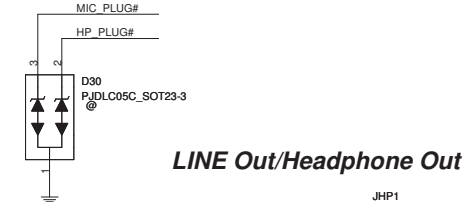
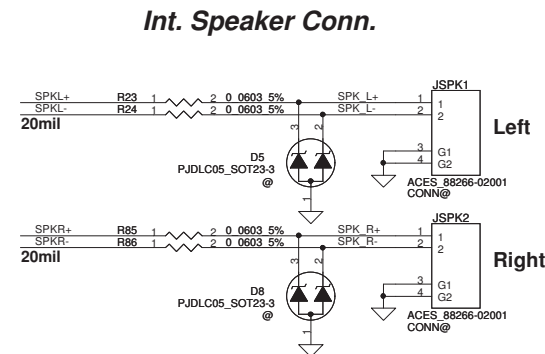
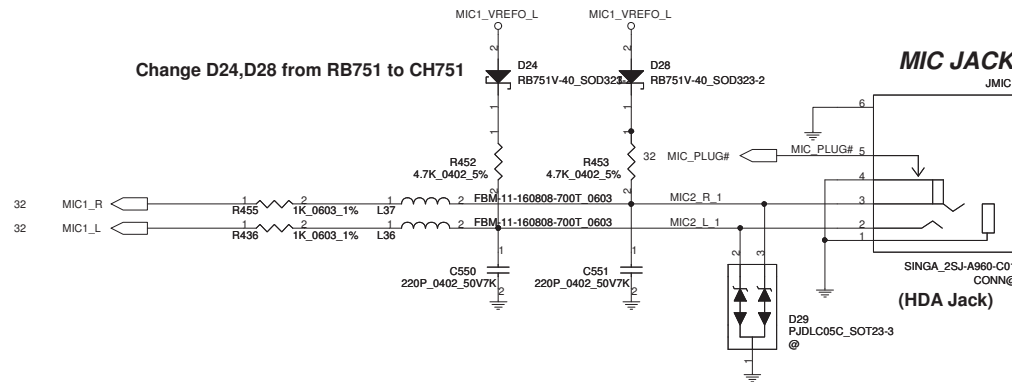
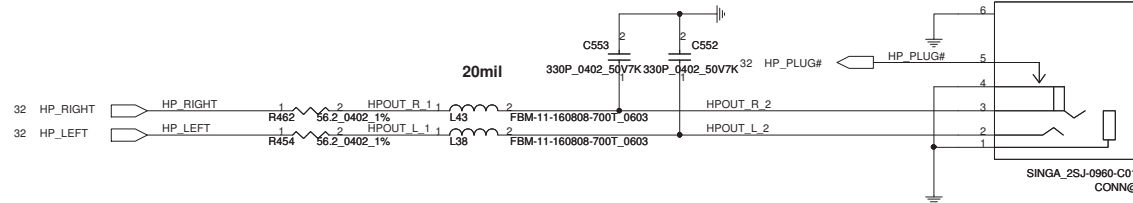
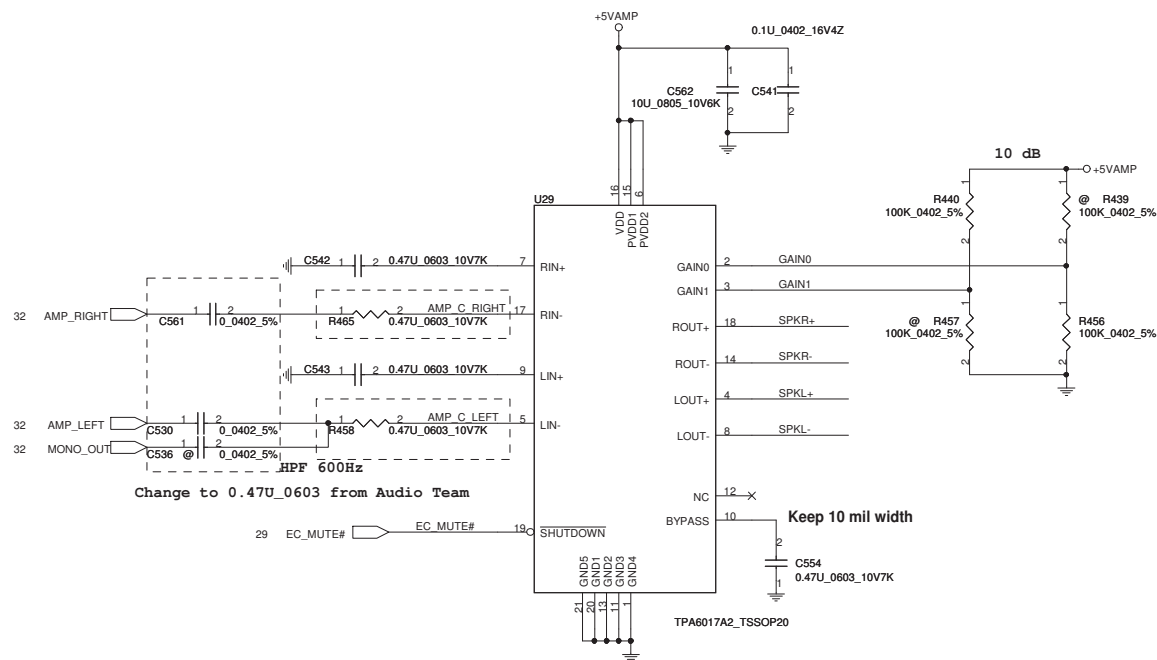
ON/OFF switch



Power ON Circuit

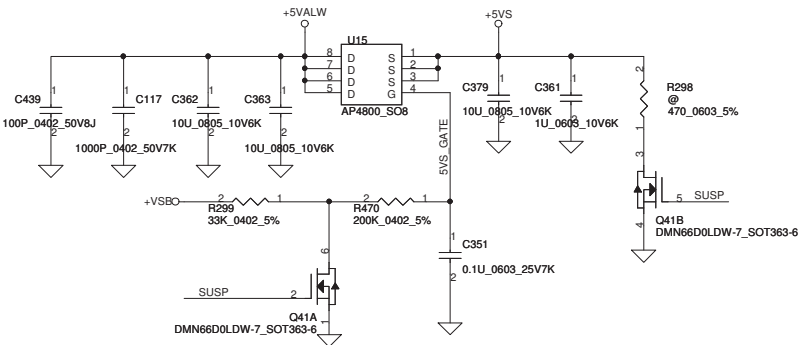


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								Document Number		PEW52 M/B LA-6634P Schematic		Rev 0.2	
								Date: Friday, August 06, 2010		Sheet 31 of 44			

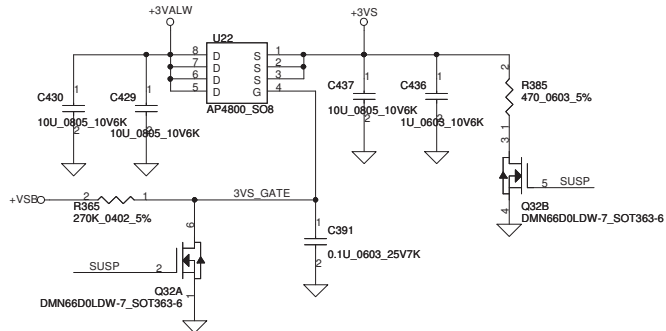


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								Date		Friday, August 06, 2010		Sheet		33 of 44	
								Rev		0.2					

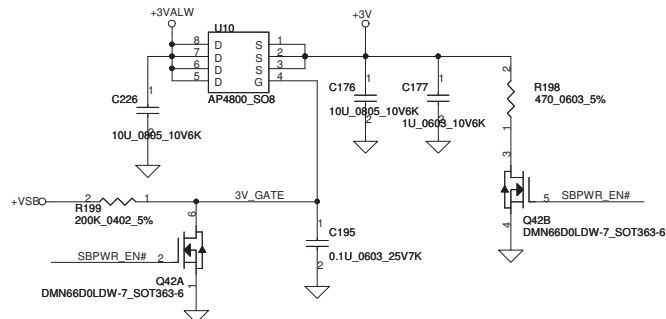
+5VALW TO +5VS



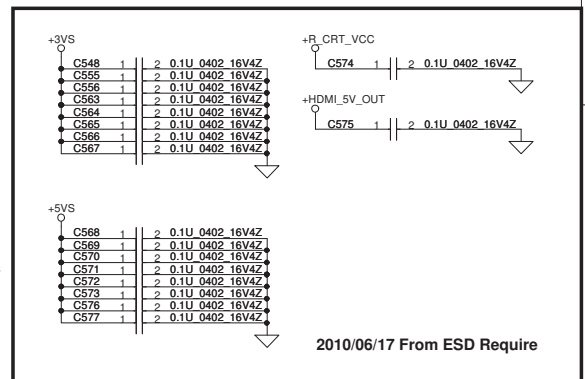
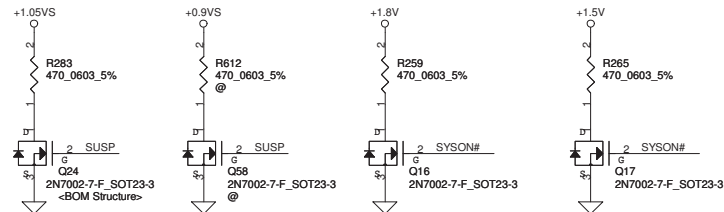
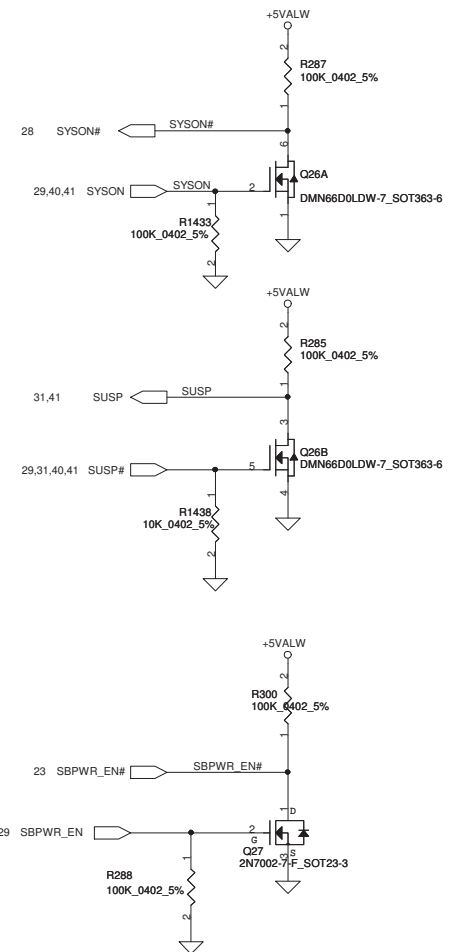
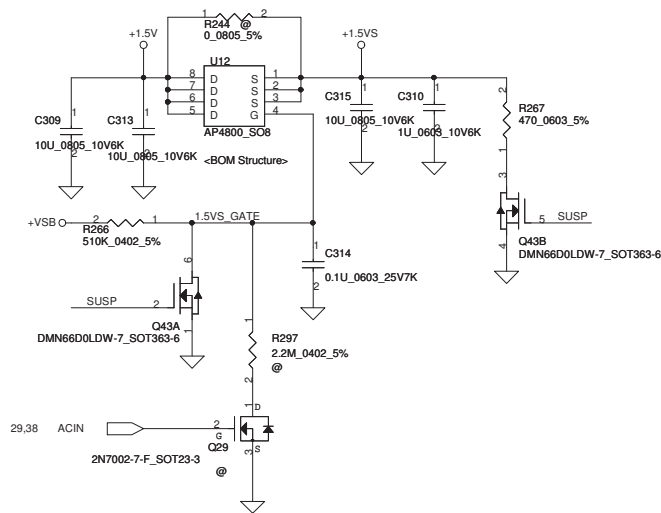
+3VALW TO +3VS



+3VALW TO +3V_SB(ICH8M AUX Power)

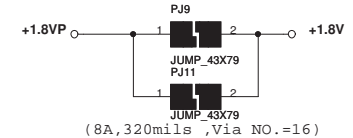
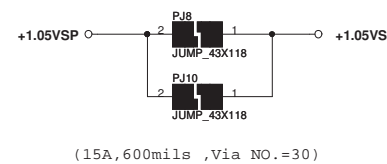
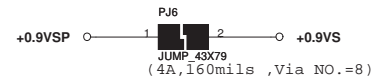
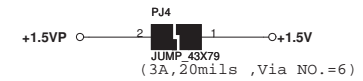
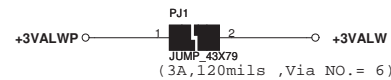
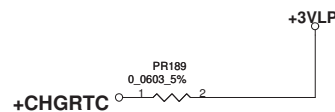
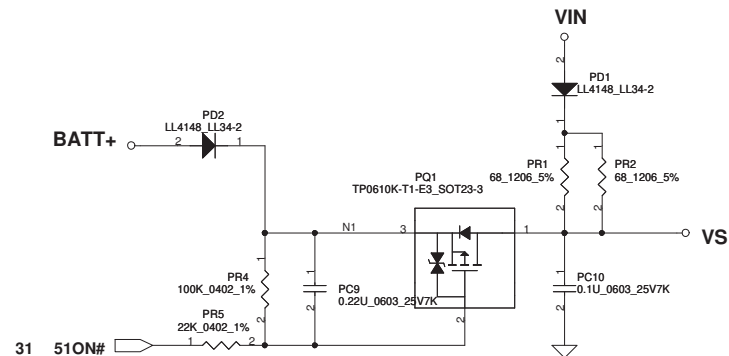
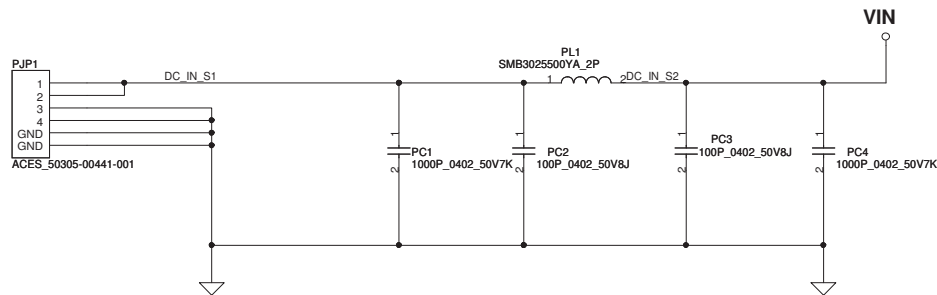


+1.5V to +1.5VS



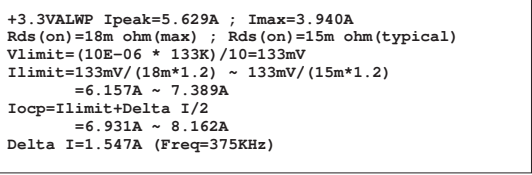
2010/06/17 From ESD Require

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Page 8				Document Number				PEW52 M/B LA-6634P Schematic			
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PL10
FBMA-L18-453215-900LMA90T_1812



```
RT8205
TONSEL=VREF      (1) SMPS1=300KHZ  (+5VALWP)
                   (2) SMPS2=375KHZ (+3VALWP)

TPS51125A
TONSEL=VREF      (1) SMPS1=245KHZ  (+5VALWP)
                   (2) SMPS2=305KHZ (+3VALWP)

3.3VALWP Delta I = 1.902A (Freq=305KHz)
Iocp = 7.108A ~ 8.34A
5VALWP Delta I = 3.199A (Freq=245KHz)
Iocp = 8.74A ~ 10.16A
```

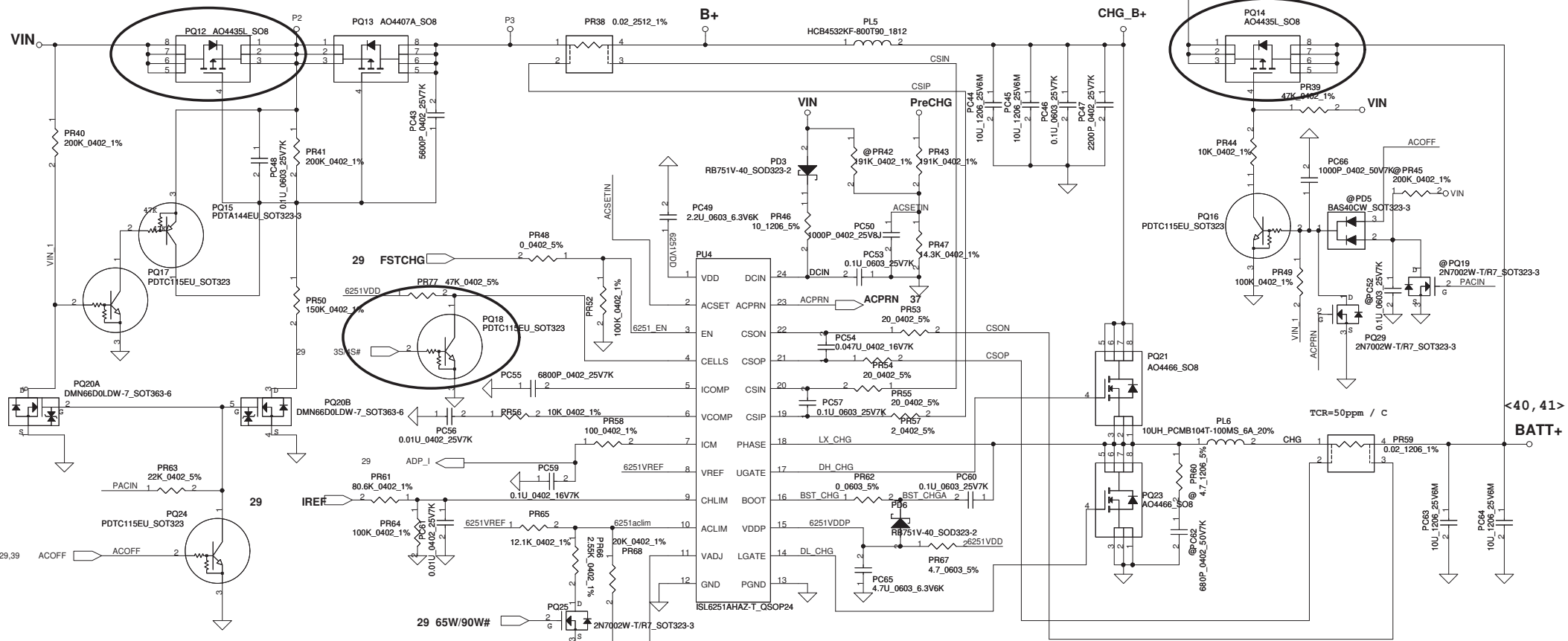
```
+5VALWP Ipeak=7A ; Imax=4.9A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(10E-06 * 154K) /10=154mV
Ilimit=154mV/(18m*1.2) ~ 154mV/(15m*1.2)
      =7.14A ~ 8.56A
Iocp=Ilimit+Delta I/2
      =8.44A ~ 9.86A
Delta I=2.613A (Freq=300KHz)
```

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I_{ada}=0~4.74A (90W/19V=4.736A)
I_{ada}=0~3.42A (90W/19V=3.421A)

ADP_I = 19.9*I_{adapter}*R_{sense}

CP = 85%*I_{ada} ; CP = 4.07A
CP = 85%*I_{ada} ; CP = 2.91A



CP mode
I_{input}=(1/0.02) (0.05*V_{ac1m}/2.39+0.05)
where V_{ac1m}=1.502V, I_{input}=4.07A

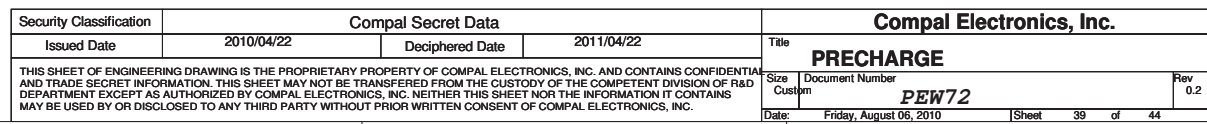
CC=0.6~4.48A
I_{REF}=0.7224*I_{charge}
K_i=0.7224
I_{REF}=0.43V~3.24V

K_i
V_{chlim}=I_{ref}*(PR374/(PR372*PR374))
=I_{ref}*(100K/(80.6K*100K))
=I_{ref}*0.5537
I_{charge}=(165mV/PR369)*(V_{chlim}/3.3V)
=(165m/20m)*(1/3.3V)*I_{ref}*0.5537
=1.3842*I_{ref}
I_{ref}=0.7224*I_{charge} => K_i=0.7224

K_v
R_{internal} ic=514K R_{ec}=3K R₁=PR379=15.4K R₂=PR381=31.6K
R=514K/(31.6K/(15.4K+3K))+11.372K
r=514K/(514K/(31.6K+28.14K))
V_{oc1}=0.175*V_{adj}+3.99V
4.2V=0.175*V_{adj}+3.99V => V_{adj}=1.2V
V_{adj}=V_{ref}*(R/(R+514K))+CALIBRATE*(r/(r+514K))
1.1483=CALIBRATE*0.6046 => CALIBRATE=1.899
1.899=(4.2-(V_{oc1}+0.175))*K_v=(4.2-(4.2+0.175))*K_v
A=V_{ref}*(R/(R+514K))+0.052
K_v=9.451

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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VFB=0.75V
 $V_o = VFB * (1 + PR97/PR98) = 0.75 * (1 + 5.9K/5.76K) = 1.8V$
 $Fsw = 282KHz$

<Vo=1.8V>
 $Fsw = 262KHz$ Cout ESR=15m ohm Rdson(max)=18m Rdson(min)=15m
 $I_{peak} = 11.3A$, $1.2I_{peak} = 13.56A$, $I_{max} = 7.91A$
 $\Delta I = ((19-1.5) * (1.5/19)) / (L * Fsw) = 2.3969A$
 $\Rightarrow 1/2 \Delta I = 1.198A$
 $V_{trip} = R_{trip} * I_{0uA} = 18K * 10uA = 0.18V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.2 + 1.198 = 12.2A$
 $I_{ocp} = 9 \sim 12.2A$

VFB=0.75V
 $V_o = VFB * (1 + PR108/PR109) = 0.75 * (1 + 12K/30K) = 1.05V$
 $Ton = 19 * e^{-12 * 143000} * ((2/3) * V_o + 100mV) / 19 + 50ns$
 $= 2.645e-7 us$
 $\Rightarrow V_o / V_{in} = D = Ton / Ts \Rightarrow Ts = 3.35us$
 $Fsw = 261KHz$ (by caculation tool)

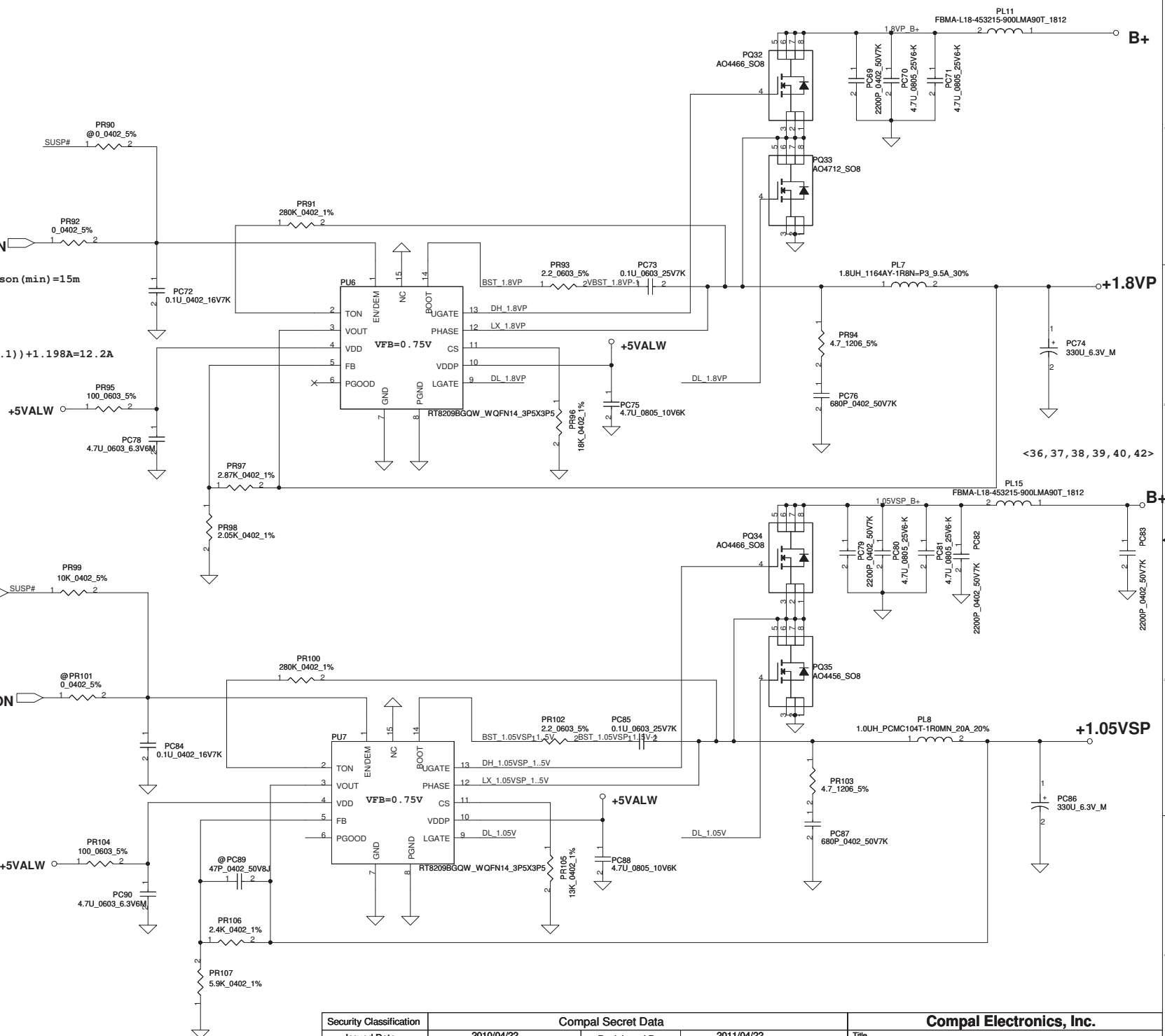
<Vo=1.05V> VFB=0.75V
 $V_o = VFB * (1 + PR108/PR109) = 0.75 * (1 + 12K/30K) = 1.05V$
 $Fsw = 261KHz$ Cout ESR=15m ohm Rdson(max.)=5.6m
 $R_{dson(min)} = 4.5m$
 $I_{peak} = 14.9A$, $I_{max} = I_{peak} * 0.7 = 10.43A$ $I_{ocp} = 17.88A$
 $\Delta I = ((19-1.05) * (1.05/19)) / (L * Fsw) = 2.11A$
 $\Rightarrow 1/2 \Delta I = 1.055A$
 $V_{trip} = R_{trip} * I_{0uA} = 13K * 10uA = 0.13V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.3 + 1.055 = 18.95A$
 $I_{ocpmax} = (0.13 / (0.004 * 1.1)) + 1.055A = 27.36A$
 $I_{ocp} = 18.95A \sim 27.36A$

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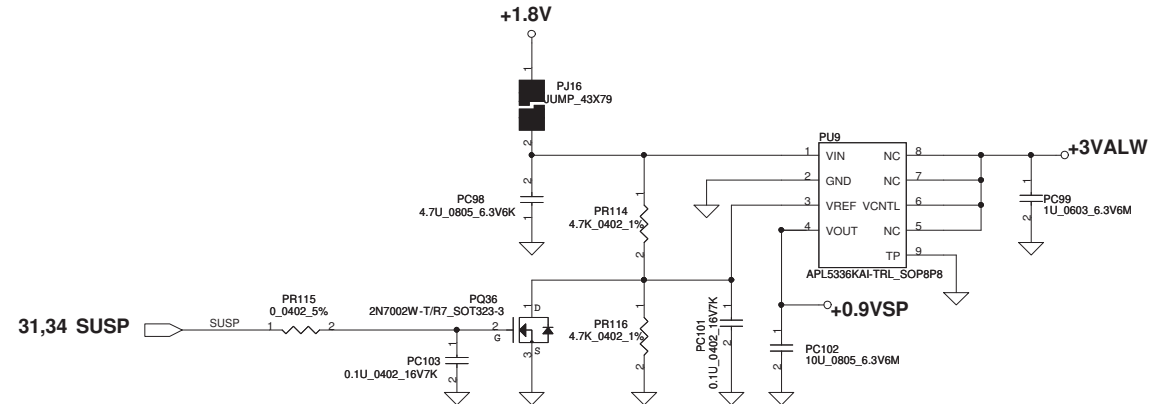
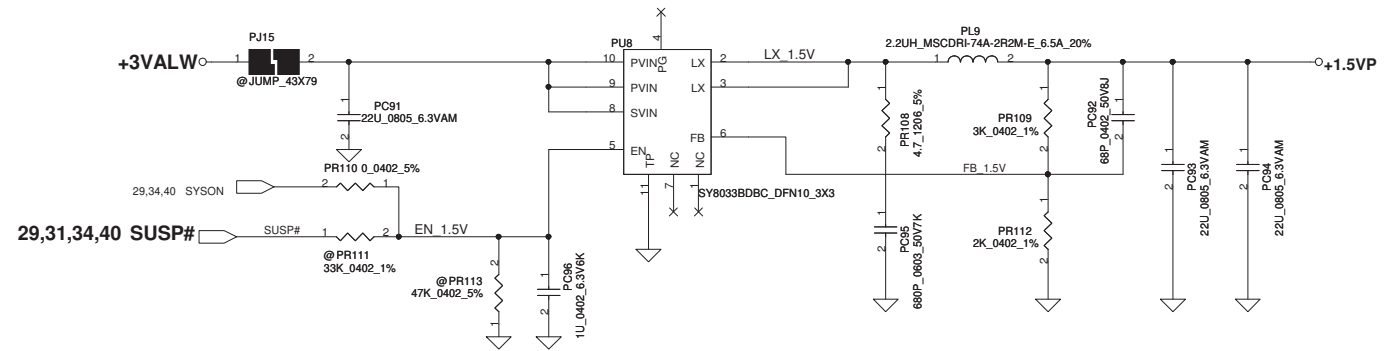
29,34,41 SYSON

29,31,34,41 SUSP#

31 VS_ON



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add 3S/4S pin function	add 4 cell battery	0.2	45	add PQ18 PDTC115EU_SOT323 (SB301150200) and PR77 47K +-5% 0402 (SD028470280)	2010/06/11	EVT
2	ACSETIN net	ACSETIN net no connect	0.2	45		2010/06/11	EVT
3	1.5V enable	1.5V enable BOM error	0.2	45	add PR92 and delete PR90 0_0402_5% (SD028000080)	2010/06/11	EVT
4	EMI issue	add boost R and snubber	0.2	45	add 3/5V 1..05V/1.5V CPU sunbber		
5							
6							
7							
8							
9							
10							
11							
12							
13							
16							
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A --> C Change List
20100806 Update Revision to 0.2

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